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IBM 1800 Data Acquisition and Control System Functional Characteristics

This manual provides basic programming and operating information for the IBM 1800 System. Included are typical application areas, Processor-Controller instruction set, digital and analog input/output, and System 1800/360 interface. The Appendixes provide hexadecimal to decimal conversion, and summary tables of the instruction set and instruction execution times.

This manual (Form A26-5918-3) is a reprint of an earlier publication; it incorporates the following Technical Newsletters:

Form	Pages	Dated
N26-0138	11, 12, 97, 98, 99, 100	10/12/65
N26-0139	iii, iv, 3, 4, 7, 8, 11, 12 13, 14, 67, 68, 68.1, 68.2	11/12/65

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CONTENTS

The ever increasing pace of technology, industry, and business continues to demand more and more reliable, up to date information. History is a good teacher... true... but its compression within the past few decades of progress has taught us that today's problems require real-time answers, not a history of past performances. Data of almost every conceivable nature—available from a myriad of sources—must be collected, analyzed, and translated into terms that can be used to optimize today's performance.

IBM's answer to the demand for real-time data acquisition, analysis, and control is the IBM 1800 Data Acquisition and Control System. The 1800 System is designed to handle a wide variety of real-time applications, process control, and high-speed data acquisition. Each system is individually tailored with modular building blocks that are easily integrated to meet specific system requirements. A large family of real-time process input/output (I/O) devices is included, such as analog input, analog output, contact sense, and contact operate; as well as data processing I/O units, such as magnetic tape, disk storage, line printer, graph plotter, card and paper tape input and output. Data is received and transmitted on either a high-speed cycle-steal basis or under program control, depending on the intrinsic data rate of the I/O device. These capabilities not only meet today's requirements, but those of the future as well.

The 1800's Processor-Controller (P-C) can be used for editing, supervisory control, direct control, or data analysis. A control and data path provides for the attachment of the IBM System/360 where more powerful supervision is required. For example, the System/360 may be used to integrate the commercial aspects of an application with the controlling operations exercised by the 1800. This multiprocessor systems capability enables the handling of real-time applications of any size or complexity.

APPLICATIONS

The 1800 is capable of accepting electrical signals, both analog and digital, from such devices as thermocouples, pressure and temperature transducers, flow meters, analytical instruments, and contacts. It provides electrical on/off and analog control signals for the customer's controlling devices. Typical applications exist in the area of process control and high speed data acquisition.

PROCESS CONTROL

Industrial processing applications are wide and varied, as are the degrees of control that individual processes may require. Some general process control application areas are:

- Primary Metals Production
- Primary Metals Finishing
- Power Generation
- Power Dispatching
- Pipeline Transmission
- Paper Production
- Glass Production
- Cement Production
- Environmental Control
- Pilot Plants
- Chemical Processes
- Petroleum Refining

The IBM 1800 Data Acquisition and Control System provides maximum flexibility in the types of process data that it can accept and the variety of output signals and data format that it can produce. Some of the degrees of control that an 1800 may exercise follow in order of complexity:

Data Gathering. Process data is gathered by the 1800 System, converted into digital information, and printed to provide: (a) operating records for accounting and supervisory purposes; or (b) a record of experimental data in process research.

Data Collection and Analysis. Process data is collected by the P-C for mathematical analysis. Current performance figures are compared with those obtained in the past, and the results are printed for process operator and management evaluation.

Data Evaluation and Operator Guidance. Process data is collected, analyzed, and evaluated with respect to previously stored guidance charts. Control instructions are than typed out for the process and control room operator, and messages and log sheets are provided for management review.

Process Study. The P-C rapidly collects the process data that is necessary for the development of a model of the process. The model is developed by using a combination of empirical techniques and observing past methods of running the process. When a more complete and more precise description of the process is required, a model is constructed by using such mathematical techniques as correlation analysis and regression analysis. The process control program is then tested on the mathematical model prior to its use on the process. Extensive operator guide information is obtained. In addition, the model represents considerable progress toward complete supervisory control.

Process Optimization. An extensive P-C program, based on the model of the process, directs the 1800 System. Process data is continuously collected and analyzed for computation of optimum operating instructions. These instructions are given to the process operator via an on-line typewriter.

Supervisory Control. The P-C communicates messages and commands to the operator and, if desired, directly to the process equipment and instrumentation. The sensors that measure process conditions are continuously monitored by the P-C. The P-C program analyzes this information and then generates the required output information.

Messages from the P-C to the operator may be displayed by several methods in the operator's working area. These messages guide the operator in adjusting the status of instruments located at the point of control. Data messages based upon visual observation of the process and its instrumentation are sent back to the P-C or the process operator. These messages are evaluated by the P-C to provide additional output, if required, for continued process operator guidance. Communication between the control room operator and the process is maintained through the P-C.

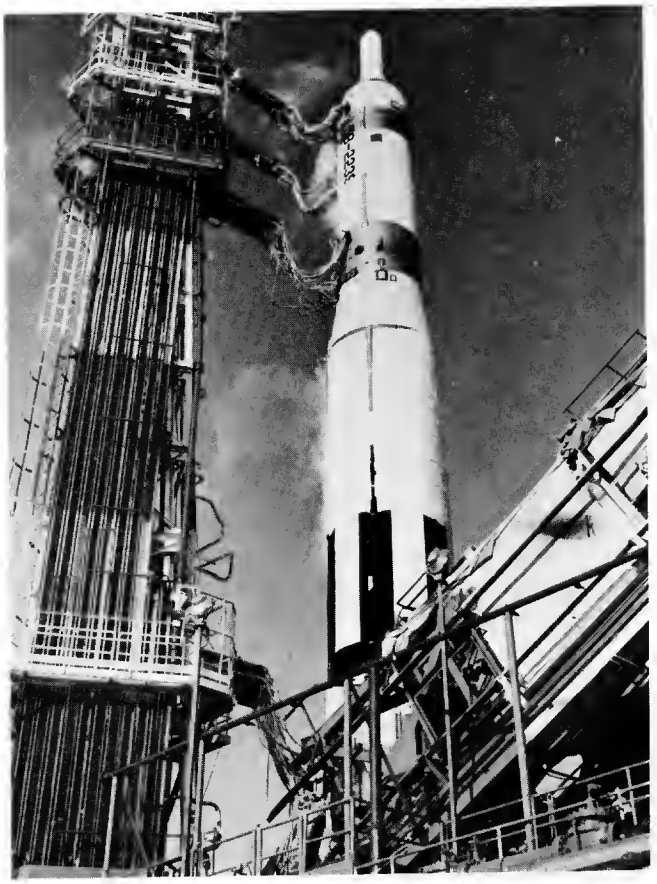
When the P-C supervisory program computes new set point values, it may—at the discretion of the operator—automatically adjust the set points of the controlling instrumentation to the new values.

HIGH SPEED DATA ACQUISITION

A High Speed Data Acquisition (HSDA) System may be thought of as a monitoring and controlling facility that is used to acquire, evaluate, and record data developed during the testing of a system (or assembly, subassembly, or component). The system here refers to anything from an anesthetized rodent in the research laboratory to a Saturn V booster on its test stand.

Many types of HSDA Systems are used. Some merely stream data directly from instrumentation to magnetic tape with a minimum of "quick look" information and data editing or checking. However, as experimental work on large systems has become more complex and time consuming, a trend has been observed toward HSDA Systems with more sophisticated data reduction and real-time display requirements. HSDA Systems most readily meet these requirements when the system design is based on a digital computer.

Many aerospace applications, for example, now require control signals to modify the test as a result of out-of-limit conditions or evaluation of sample test data. Thus we find a direct parallel with the historical development of process Control Systems. They began with data gatherings; progressed to operator guide control; and, where the applications required it, automatically applied system output commands directly to the process equipment.



The following are typical HSDA application areas for the 1800 System:

*Note: The illustrations in this manual have a code number in the lower corner. This is a publishing control number and is unrelated to the subject matter.

Missile Check Out
Wind Tunnels
Static Test Stands
Missile Telemetry
Nuclear Reactor Research
Particle Physics Control and Acquisition
Environmental Chambers
Flight Simulators
Hybrid Systems
Medical Research
Medical Analysis—Clinical

OTHER ACQUISITION AND CONTROL

The 1800 System has been designed to handle widely divergent applications which involve real-time processing abilities. Inputs may include signals from only digital sources or from both digital and analog sources. If desired, the results of analyzing the required data may be displayed in analog or digital form, or used to cause direct functions.

These applications cover a wide range, including the following areas:

General Research
Traffic Control (vehicle, railways, etc.)
Engine Testing
Component Testing
Quality Control
Information Display
Material Dispatching
Marine Operating Systems

SYSTEM DESCRIPTION

Components of the IBM 1800 Data Acquisition and Control System can be used in three basic configurations:

1. The 1800 System process I/O equipment attached to the Processor-Controller, with any necessary data-processing I/O units. The minimum system will satisfy initial control and analysis needs and can be expanded to support medium-scale applications.
2. The 1800 System process I/O equipment attached directly to a System/360, Model 30, 40, or 50. This configuration is well suited to medium-scale, real-time applications involving substantial data processing loads.
3. One or more 1800 Systems (Processor-Controllers, each with appropriate process I/O equipment) attached via channel adapters to a System/360. This configuration is suited to large-scale, real-time applications, and can be expanded to supply almost any combination of data processing capability and real-time input/output channel capacity.

PROCESSOR-CONTROLLER (P-C)

- Central Processing Unit provides arithmetic, logic, and control functions for the 1800 System.
- Stored program controls input/output and processing.
- Standard features include three Index Registers, 12 levels of Priority Interrupt, three Data Channels, three Interval Timers, an Operations Monitor, and an Operator's Console.
- Design includes basic circuitry and controls for attachment of process input/output equipment.

The Processor-Controller contains a small, binary, stored-program Central Processing Unit (CPU). Within its basic design, it has interrupt and cycle-stealing capabilities which are used in controlling the various I/O devices to be attached by the using system. Index Registers and Indirect Addressing are provided to facilitate address modification and programming.

While the instruction set is limited to 31 discrete instructions, the computer has very high performance for tasks normally encountered in data acquisition and control applications.

Two Processor-Controllers are available: the IBM 1801 and the IBM 1802. Each has eight models based on speed and size of the core storage. The 1801 has no provision for magnetic tape, while the 1802 includes the Tape Adapter Unit for the 2401 and 2402 Magnetic Tape Units.

The System/360 Adapter is available as a special feature of the Processor-Controller to link together the 1800 System and the System/360 Model 30, 40 or 50. With this feature, data can be transferred from one system to the other on a channel-to-channel basis.

PROCESS INPUT/OUTPUT FEATURES

- Modular features are available to match the 1800 System with the process requirements.
- Analog Input converts bipolar voltage or current signals to digital values for use by the computer.
- Digital Input accepts binary information represented by contact closures or voltage levels.
- Analog Output converts digital values to precise voltage levels for operating process devices.
- Digital Output provides binary data to the process in the form of "contact" closures or voltage levels.

Analog Input features include analog-to-digital converters, multiplexers, amplifiers, and signal conditioning equipment to handle all types of process analog input signals. System conversion rates to 20,000 samples per second are provided, with program selectable resolution and external synchronization. Analog input capacities are 1,024 relay multiplexer points and 256 solid-state (high-speed) multiplexer points. A second analog-to-digital converter can be added to double system analog input performance and capacity.

The Digital Input features provide up to 384 process interrupt points; up to 1,024 bits of contact sense, digital input, high-speed parallel register input; or 128 high-speed pulse counters.

Analog Output features provide up to 128 analog output points for individual or simultaneous operation of a wide range of customer devices.

The Digital Output features provide up to 2,048 bits of pulse output, electronic "contact" operate, and high-speed register output.

DATA PROCESSING I/O UNITS

- Adapters and controls are available for attaching a wide variety of Data Processing I/O Units.

Data Processing I/O Units function with an external document such as a punched card or a reel of magnetic tape. To provide the logical and buffering capabilities necessary for operation on the 1800 System, a control (adapter) feature is available for each I/O Unit.

The following I/O Units can be attached to the 1800 System via the Data Processing I/O attachment features:

1816 Printer-Keyboard (Modified SELECTRIC®)
1053 Printer
1442 Card Read Punch
1054 Paper Tape Reader
1055 Paper Tape Punch
1443 Printer
1627 Plotter
2310 Disk Storage
2401/2402 Magnetic Tape Unit

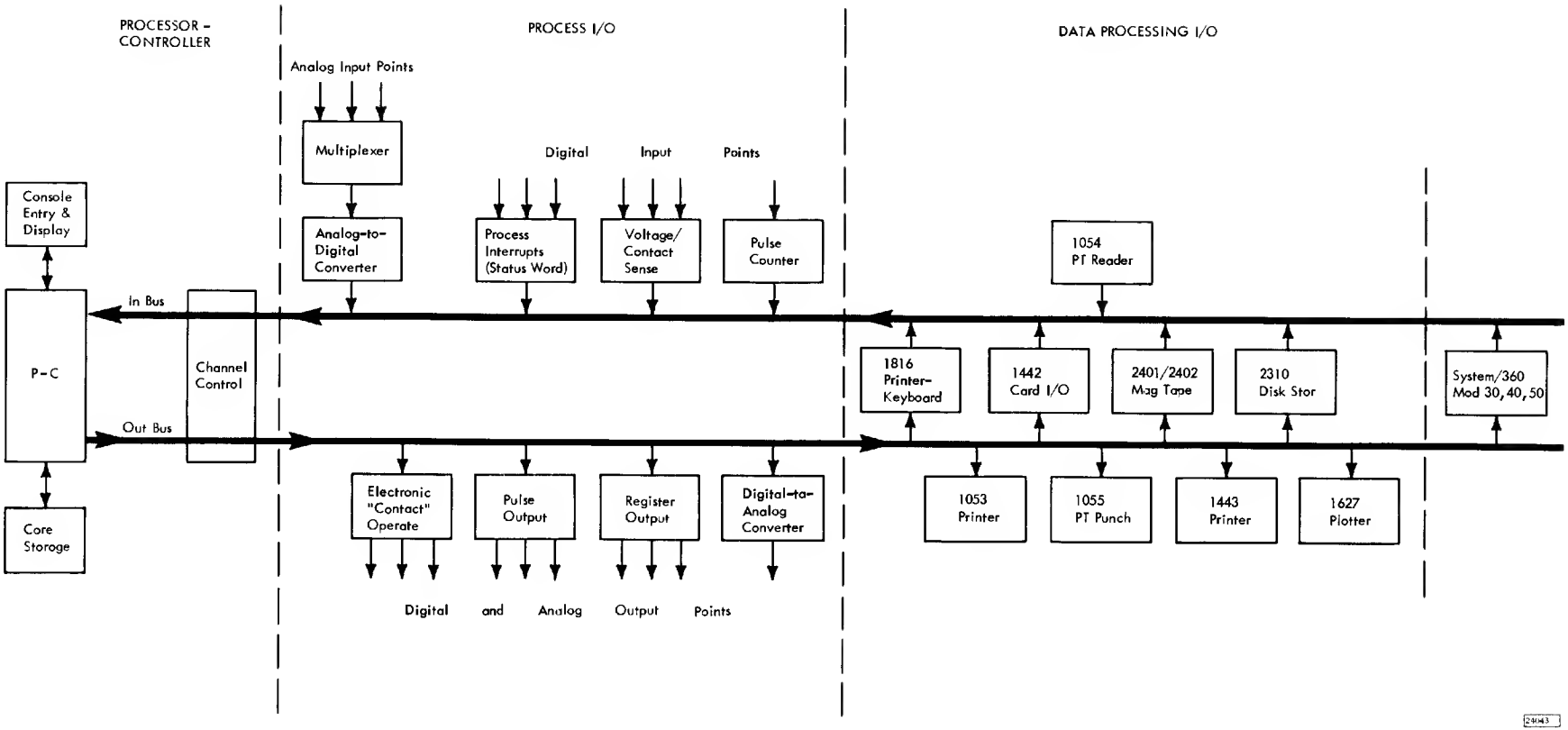
SYSTEM DATA FLOW

- Data is stored and processed in fixed-length 18-bit words for fast parallel manipulation of data.
- The I/O devices are linked to the Processor-Controller via a standard I/O interface.
- Adapter circuitry at each I/O device performs the necessary conversion, buffering, and control functions.
- Cycle-stealing capability permits high-speed transfer of data.

A standard I/O interface is used between the Processor-Controller (P-C) and all input/output devices. Adapter circuitry to accommodate each type of I/O device is installed in the 1800 System as required. The adapters provide the necessary buffer registers and controls to permit operation on the system.

Configuration 1 shows the data flow between the P-C and the various I/O devices. In a closed-loop system, process conditions are monitored and analyzed continuously, and controlling signals are sent to the devices that control the process. Input data is obtained directly from measuring devices in the process area without the need for off-line conversion equipment. Electrical signals are accepted in analog or digital form from such devices as thermocouples, pressure transducers, digital voltmeters, and contacts. Signal conditioning, multiplexing, and conversion functions are performed by the input circuits. The input data, in 1800 System format, is held in registers until called for entry into core storage.

After the input data has been read and analyzed by the Processor-Controller, the program may



Configuration 1. IBM 1800 Data Acquisition and Control System

select a process control function. Both digital and analog output data can be generated for controlling equipment such as set-point positioners, displays, and telemetry systems. Data processing information can be entered and retrieved in a variety of forms through the DP I/O units and their adapter circuitry.

When a Process I/O device or a DP I/O device is ready to send or receive data, it can notify the Processor-Controller by issuing an interrupt request. The program identifies the source of the interrupt by sensing the status of indicators associated with each I/O device. The P-C responds to the interrupt by sending the appropriate I/O command to the device. Each I/O command always places a control word on the Out-Bus to specify the input/output device and the function to be performed. Depending on the intrinsic data rate of the I/O device receiving the control word, the transfer of data between core storage and the device can take place under direct program control, or on a Data Channel operation. A Data Channel transfers data on a high-speed cycle-steal basis, using a data table in core storage for flexibility of scanning rates and patterns. The cycle-stealing capability makes it possible to delay the program for one machine cycle and to use this cycle to transfer the data word between P-C storage and the I/O device. Cycle-stealing and interrupt servicing are conducted by the P-C on a priority basis. This makes it possible to simultaneously control combinations of real-time input/ouput devices.

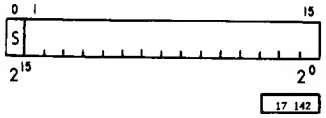
A brief description follows of 1800 features and units that will facilitate an understanding of the P-C instruction set. More detailed descriptions are provided at appropriate sections of the manual. The data processing I/O units (card, paper tape, etc.) are described in the 1800 Data Processing I/O Manual (A26-5969).

PROCESSOR-CONTROLLERS

The Processor-Controllers (1801 and 1802 models), are fixed-word-length, binary computers. Four memory sizes are available — 4, 8, 16, or 32K words of 18 bits each — with memory cycle times of 2 or 4 microseconds (μsec). Two of the 18 bits are used for (1) storage protection and (2) parity check. There are 16 data bits in each word. A repertoire of 31 instructions (many of which serve multiple functions) includes arithmetic instructions that manipulate both 16-bit and 32-bit words (16 data bits are handled in parallel). The 2 μsec system can perform high-speed I/O operations during cycle steal operations via Data Channels at rates up to 500,000 words (or 8,000,000 bits) per second in burst mode. Both indirect addressing and index registers (3) are provided for address modification. Other P-C features include a multi-level interrupt system, three high-resolution interval timers, storage protection, an auxiliary storage for on-line diagnostics, operations monitor, and an operator's console.

Data Representation

The standard or single precision data word is 16 bits in length.



Positive numbers are always in true binary form, whereas negative numbers are in two's complement form. The sign bit (position 0) is always 0 for positive numbers and 1 for negative numbers. The 2's complement of a binary number is defined as its 1's complement increased by one. The 1's complement of a binary number is that number that results by replacing each 1 in the number with a 0 and each 0 with a 1. The decimal numbers are shown in Figure 1 with their binary equivalents and 1's and 2's complements:

Decimal	Binary	1's Comp	2's Comp
15	01111	10000	10001
9	01001	10110	10111
3	00011	11100	11101

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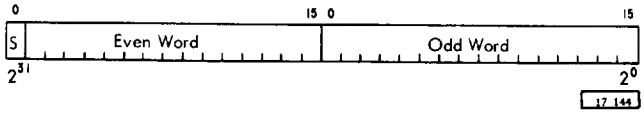
Figure 1. Binary 1's - 2's Complement

Bit positions 1 through 15 represent decimal values of 2^{14} through 2^0 respectively. Thus the largest single precision positive number that can be represented is $2^{15} - 1$ or 32,767 (a sign bit of 0 and 1's in all other bit positions). The largest negative number is -2^{15} or −32,768 (a sign bit of 1 and 0's in all bit positions). The number zero is represented by all bits being zero. There is no negative zero.

A double precision number of 32 bits can be used to give a number range from +2,147,483,647 to −2,147,483,648 ($2^{31}-1$ to -2^{31}). Two adjacent words must be used in memory with the left-most word at an even address and the right-most word at the next higher odd address.



CORE STORAGE

Core storage sizes of 4096, 8192, 16,384 or 32,768 words are available. Storage cycle times — that is, the time required to transfer a word to or from a memory address — of 4 or 2 μsec are available.

Each word consists of 18 bits: 16 are data bits which can be either data or instructions; one bit is used for the Storage Protect feature; one bit is used for odd bit parity. Parity includes the 16 data bits and the Storage Protect bit. The parity bit cannot be affected by the program. Detection of a parity check causes an interrupt to the internal interrupt level. See Interrupt section.

Core storage addresses 0004, 0005, 0006 are reserved for the Interval Timers; addresses 0008 through 0034 are reserved for interrupt addresses.

Addressing

Core storage addresses begin at 00000 and end at 4095, 8191, 16,383 or 32,767 depending on storage size. Storage wrap around exists; that is, the next sequential address above the highest numbered address is always 00000.

Although core storage addresses have been expressed in decimal (base 10) form up to now, the 1800 P-C is binary (base 2) form. Internal addressing and console displays are in 16-bit binary form. For example.

4095_{10} equals 0000111111111111_2
8191_{10} equals 0001111111111111_2
$16,383_{10}$ equals 0011111111111111_2
$32,767_{10}$ equals 0111111111111111_2

Greater ease of operation is realized when hexadecimal (base 16) representation is used. Programming Systems for the 1800 make use of this notation. A description of binary and hexadecimal number systems is provided in the Number Systems section.

Arithmetic

The arithmetic operations of the P-C include add, subtract, multiply, compare, and divide. Negative data is always stored and operated upon in 2's complement form. Addition, subtraction, and compare can be done in single or double precision. Multiplication operates on two single precision words to provide a double length product. Division allows the dividend to be double length and uses a single precision divisor to provide a single precision quotient and a single precision remainder.

Overflow and Carry Indicators

The two indicators associated with the Accumulator are Overflow and Carry. The Overflow indicator can be turned on by add, subtract, or divide, and indicates a result larger than can be represented in the Accumulator. Once Overflow is on, it will not be changed except by testing the indicator, or by a Load Status or Store Status instruction. The Carry indicator provides the information that a "one" is to be carried or borrowed from the next higher precision word when extended precision arithmetic is performed by programming. The Carry indicator is dynamic and changes with each add or subtract operation. The Carry indicator is also affected by shift instructions.

Indirect Addressing

Indirect addressing is a standard feature of the 1800. One level of indirect addressing is provided. Except for the MDX instruction with T=00, indirect addressing cannot be used with one word instructions. The instructions that can be modified by indirect addressing are indicated in Table 2. (See Instruction Set section.) The recognition in the instruction of an Indirect Address Control bit (position 8, two-word instruction only) will cause the address portion to be treated as an indirect address. The address after indexing (if specified) gives the location of the effective address. An additional memory cycle is required.

Index Registers

Three index registers (XR) are standard features. The XR's are addressed by the TAG (positions 6 and 7 in the instruction), as follows:

Bits 6 & 7	XR
01	1
10	2
11	3

Operations on the XR, such as load, store, modify and skip, will be accomplished through instructions in the basic instruction set. The contents of an Index Register or the Instruction Register are usually used to perform address arithmetic.

Data Channels

Data Channels give the P-C the ability to delay the execution of a program while an I/O device communicates with core storage. For example, if an input unit requires a memory cycle to store data that it has collected, the data channel with its "cycle stealing" capability makes it possible to delay the program during execution of an instruction and store the data word without changing the logical condition of the P-C. After the data is stored, the P-C continues executing the program which was delayed by the "cycle-stealing." This capability should not be confused with interrupt which changes the contents of the Instruction Register.

Cycle stealing by the Data Channels can occur at the end of any memory cycle. Maximum delay before cycle stealing can occur is 2.25 μs for the 2 μs system and 4.5 μs for the 4 μs system.

A WAIT instruction, which halts the P-C, will not stop the operations of Data Channels.

Interrupt

The interrupt facility provides an automatic branch in the normal program sequence based upon external conditions (those in the process) or internal conditions (those within 1800). Examples of such conditions are:

- The detection of an external process condition that requires immediate attention.
- A P-C Interval Timer has concluded the recording of a preset time interval.
- A magnetic tape drive has completed a data transfer previously requested and is ready for another request.
- An operator has initiated an interrupt from the P-C console.

These devices and conditions are assigned priority levels by the user. An interrupt request will not be honored while the level of the request itself or any higher level is being serviced. A request will be honored if no interrupt is being serviced or if any lower level than that of the request is being serviced. A Wait instruction will not prevent interrupts from being serviced.

INSTRUCTION FORMATS

Two basic instruction word formats are used (Figures 2 and 3). The bits within the instruction words are used in the following manner:

OP	These five bits define which operation is to be performed by the P-C.
F	This format bit controls the instruction format. A "zero" indicates a single word instruction and a "one" indicates a two word instruction.
T	These two Index Tag bits address the Index Register or Instruction Register (I) used in the address modification.

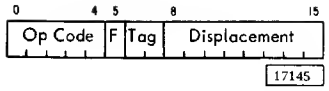


Figure 2. One-Word Instruction Format

DISP	These eight bits are called the displacement and, with one word instructions only, are usually added to the Instruction Register or the index register specified by T. The modified address is defined as the effective address (EA). If T is 00, the displacement is added to the Instruction Register. The displacement is in 2's complement form if negative, with the sign in bit 8. The bit in position 8 is automatically extended to the higher ordered bits (0-7) when the displacement is added to an index register.
IA	Except for the Modify Index and Skip instruction with T=00, the Indirect Addressing bit is used in the two word instruction format. If "zero", addressing will be direct. If a "one", addressing will be indirect.
BO	This bit is used to specify that the Branch or Skip on Condition (BSC) instruction is to be interpreted as a "Branch Out" when used in an interrupt routine.
COND	Specifies the condition of indicators that are interrogated on a BSC or BSI instruction.
ADDRESS	These 16 bits usually specify a core storage address in a two word instruction. The address can be modified by the contents of an index register or used as an indirect address if the IA bit is on.

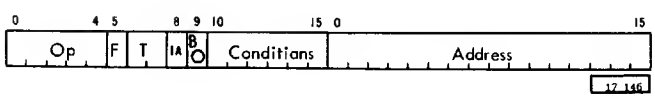


Figure 3. Two-Word Instruction Format

Table 1. Determining Effective Addresses

	F = 0 (Direct Addressing)	F = 1, IA = 0 (Direct Addressing)	F = 1, IA = 1 (Indirect Addressing)
	(1) (2)		(3)
T = 00	EA = I+Disp	EA = Address	EA = C (Address)
T = 01	EA = XR1+Disp	EA = Address+XR1	EA = C (Address+XR1)
T = 10	EA = XR2+Disp	EA = Address+XR2	EA = C (Address +XR2)
T = 11	EA = XR3+Disp	EA = Address +XR3	EA = C (Address+XR3)

(1) Contents Of Instruction Register Or Index Register.
(2) May Be True Positive Quantity Or Negative 2's Complement Quantity.
(3) C Specifies "Contents" At Locotion Specified By Address or Address +XR1, 2, or 3.

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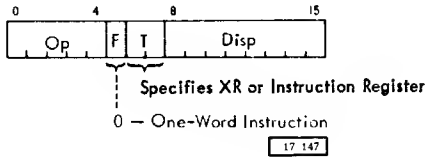
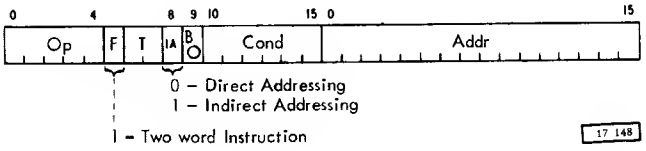
Effective Address Generation

The effective address (EA) is developed as shown in Table 1 for most instructions (exceptions are noted in the Instructions section).





P-C REGISTERS

The following registers are used in the manipulation of data within the P-C and may be displayed on the P-C console.

Storage Address Register (SAR)

All P-C program references to storage are under direct control of this 16-bit register. Data Channel (DC) references to storage use the Channel Address Register (CAR) of the active DC. See Data Channel section.

Instruction Register (I)

This 16-bit counter register holds the address of the next sequential instruction. It is automatically incremented for sequential operation of instructions.

Storage Buffer Register (B)

This 16-bit register is used for buffering all word transfers with core storage.

Arithmetic Factor Register (D)

This 16-bit register is used to hold one operand for arithmetic and logical operations. The Accumulator provides the other factor.

Accumulator (A)

This 16-bit register contains the results of any arithmetic operation. It can be loaded from or stored into core storage, shifted right or left, and otherwise manipulated by specific arithmetic and logical instructions.

Accumulator Extension (Q)

This register is a 16-bit low order extension of the Accumulator. It is used during multiply, divide, shifting, and double precision arithmetic.

Shift Control Counter (SC)

This six-bit counter is used primarily to control shift operations.

OP Register (OP)

This five-bit register is used to hold the operation code portion of an instruction.

NOTE: The above registers are also used uniquely in specific operations described later.

P-C DATA FLOW

As shown in the simplified P-C Data Flow block diagram (Figure 4), all instructions and data entering and leaving core storage do so via the B-register. Input devices send data and instructions to the B-register via the In-Bus. Output devices receive data from the B-register via the Out-Bus. As each stored program instruction is selected, its various parts (op code, format bit, etc.) are directed to the Control registers via the B-register and the Out-Bus. The Control registers decode and interpret each instruction before the instruction is executed.

Except for Data Channel operations (see I/O Control section), all instructions and data must first be addressed by the Storage Address Register (SAR) before leaving core storage. SAR obtains the core storage address from the I-register or the A-register. The contents of the I-register are developed by one of the following means, depending on the P-C operation:

1. The I-register is incremented for each instruction during sequential operation of the stored program instructions.
2. The effective address of each instruction is developed in the accumulator (A-register) and then transferred to SAR. The contents of the accumulator are saved in an auxiliary register during effective address computation. If the instruction was a branch, the contents of SAR is transferred to the I-register.

Data Transfer, 18 Bits

Each word in core storage comprises 18 bits: 16 data bits, a parity bit (P), and a storage protect bit (S). During P-C operation, the P bit is automatically added or removed to maintain odd parity. The S bit is added or removed by the Store Status instruction, depending on whether a "read only" condition is desired. The 16 data bits enter or leave core storage via the B-register. The P and S bits do so via

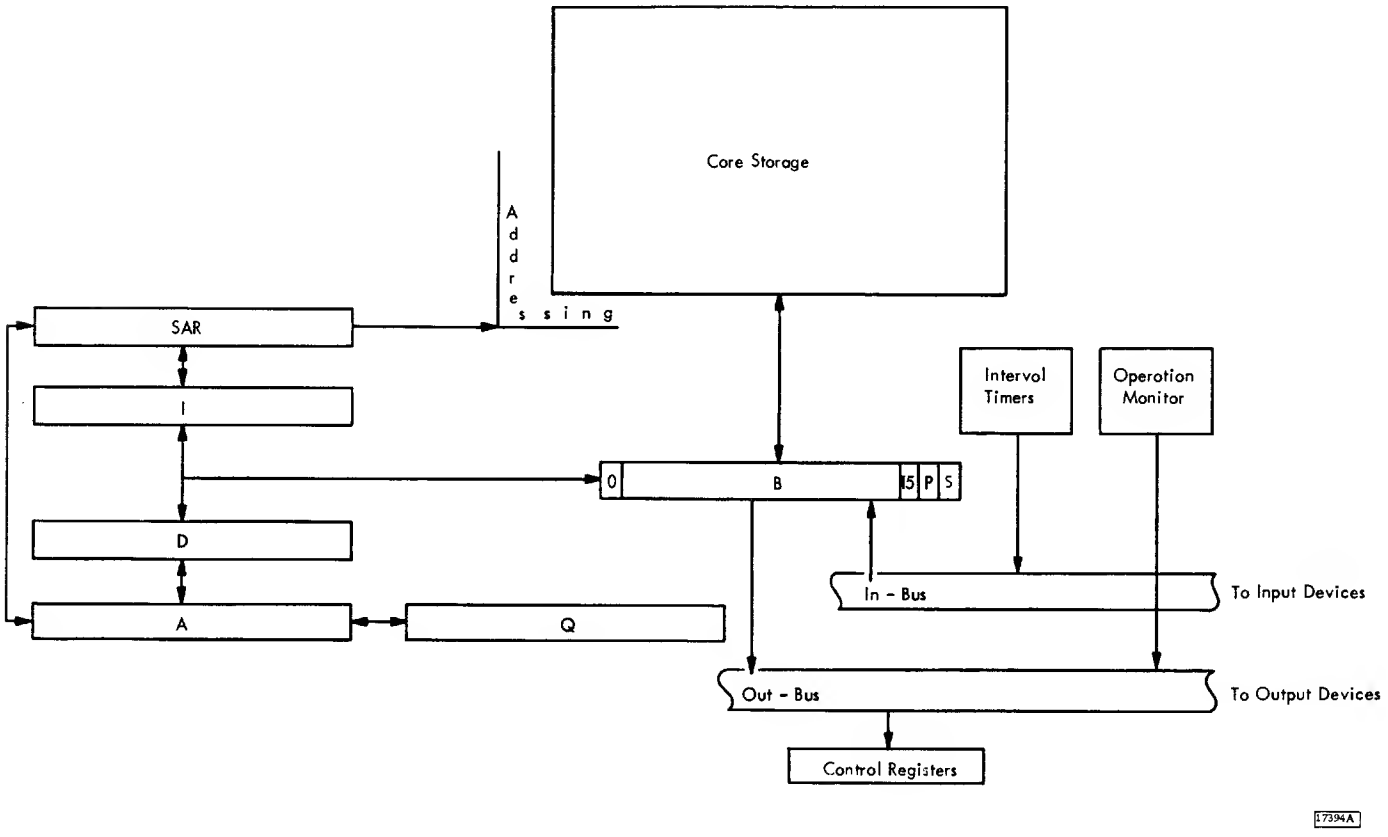


Figure 4. 1800 P-C Data Flow

individual latches. The latches and the B-register together enable the transfer of 18 bits to and from core storage. The In-Bus and the Out-Bus contain 16 data lines and 2 parity lines. Thus, 18 bits can be transferred between the P-C and the magnetic tape units. (See "Data Formats" in the magnetic tape units section of the 1800 I/O manual, A26-5969.)

NUMBER SYSTEMS

This section is provided for those unfamiliar with binary and hexadecimal number systems. By way of review, it is well to remember that in any number system no single integer can exceed the value of the number system less one. For example, nine is the largest integer that can exist in any decimal or base 10 number; one is the largest integer that can exist in any binary or base two number; and the integer representing 15 (F) is the largest value integer that can exist in any hexadecimal or base 16 number.

It is also well to remember that any number can be expressed in powers of its base number. For example, 1375_{10} can be expanded or expressed as

$$1 \times 10^3 + 3 \times 10^2 + 7 \times 10^1 + 5 \times 10^0$$

or

$$1000 + 300 + 70 + 5$$

(Any number to the zero power equals one.)

Binary

Binary data consists of two digits, zero and one. Thus, the decimal digits 0 through 9 are expressed in binary form, as follows:

DECIMAL	BINARY	DECIMAL	BINARY
0	0000	5	0101
1	0001	6	0110
2	0010	7	0111
3	0011	8	1000
4	0100	9	1001

Note that a one in the rightmost position of the binary number is equivalent to a decimal one; a one in the second position is equivalent to a decimal 2; a one in the third position, to a 4; a one in the fourth position, an 8; if there was a fifth position, a one in that position would be equivalent to 16; a one in the sixth, 32, and so on. The decimal equivalent of each position is twice that of the position to its right.

Hexadecimal

Hexadecimal data are expressed to the base 16 and are related to the decimal numbers as follows:

Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexadecimal	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Thus, hexadecimal numbers proceed from 0 through F (0 through 15 decimal), 10 through 1F (16 through 31 decimal), 20 through 2F (32 through 47 decimal), etc.

Binary to Hexadecimal Conversion

Binary numbers can be separated into four-position groups for conversion to hexadecimal. For example, the binary number 010101011111 can be separated as follows:

$$\underset{5}{\underline{0101}} \qquad \underset{5}{\underline{0101}} \qquad \underset{F}{\underline{1111}}$$

Thus,

$$010101011111_2 = 55F_{16}$$

Hexadecimal to binary conversion is, of course, simply the reverse of binary to hexadecimal. For example, the hexadecimal number 1FFF equals 0001111111111111_2 ($F_{16} = 15_{10} = 1111_2$):

$$\underset{0001}{\underline{1}} \quad \underset{1111}{\underline{F}} \quad \underset{1111}{\underline{F}} \quad \underset{1111}{\underline{F}}$$

Hexadecimal to Decimal Conversion

Hexadecimal numbers can be converted to decimal numbers by expanding each position in the manner previously shown. For example,

$$\begin{aligned} 55F_{16} &= 5 \times 16^2 + 5 \times 16^1 + 15 \times 16^0 \\ &= 5 \times 256 + 5 \times 16 + 15 \times 1 \\ &= 1280 + 80 + 15 \\ &= 1375_{10} \end{aligned}$$

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000-	0000	0001	0002	0003	*0004	0005	0006	0007	*0008	0009	0010	0011	0012	0013	0014	0015
001-	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
002-	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
003-	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
004-	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
005-	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
006-	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
007-	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
008-	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
009-	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
00A-	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
00B-	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
00C-	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
00D-	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
00E-	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
00F-	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255
010-	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
011-	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
012-	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
013-	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
014-	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
015-	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
016-	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
017-	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
018-	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
019-	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
01A-	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
01B-	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
01C-	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
01D-	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
01E-	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
01F-	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511

* Core Storage locations 0004 to 0006 and 0008-0034 (Decimal addresses) are reserved for the Interval Timers and the Interrupt Addresses, respectively.

17 150

Figure 5. Hexadecimal-Decimal Conversion

Appendix A is a table for the conversion of hexadecimal to decimal and vice versa. It is partly reproduced here (Figure 5) for explanatory purposes. Note that the decimal number 0489 is boxed in the table and that the two high-order hexadecimal numbers found to the extreme left are 1E. The low-order hexadecimal number 9 is found above ($0489_{10} = 1E9_{16}$). Note also that the binary representation is shown above the table as it would appear in a console register (0000000111101001).

Thus, from the table in Figure 5, it can be seen that the hexadecimal numbers 1F0 and 1FF equal the decimal numbers 496 and 511. Or, starting from inside the table again, the decimal numbers 50 and 63 equal the hexadecimal numbers 32 and 3F.

The 1800 instruction set is made up of 31 individual instructions (00000 is an invalid code which enables the programmer to detect an inadvertent branch to a blank area of core storage). Each instruction falls into one of five classes (Table 2). Note that the instructions which may be modified with indirect addressing are indicated in the Indirect Addressing column. Some instructions perform multiple uses, as specified by their control bits. A more complete breakdown of instructions, including hexadecimal representations, is found in Appendix B. Execution times are provided in Appendix C.

Table 2. Instruction Set

Class	Instruction	Indirect Addressing	Mnemonic
Load and Store	Load Accumulator	Yes	LD
	Double Load	Yes	LDD
	Store Accumulator	Yes	STO
	Double Store	Yes	STD
	Load Index	Yes	LDX
	Store Index	Yes	STX
	Load Status	No	LDS
	Store Status	Yes	STS
Arithmetic	Add	Yes	A
	Double Add	Yes	AD
	Subtract	Yes	S
	Double Subtract	Yes	SD
	Multiply	Yes	M
	Divide	Yes	D
	Compare	Yes	CMP
	Double Compare	Yes	DCM
	And	Yes	AND
	Or	Yes	OR
	Exclusive Or	Yes	EOR
Shift	Shift Left Instructions		
	Shift Left Logical (A) *	No	SLA
	Shift Left Logical (AQ) *	No	SLT
	Shift Left and Count (AQ) *	No	SLC
	Shift Left and Count (A)	No	SLCA
	Shift Right Instructions		
	Shift Right Logical (A) *	No	SRA
	Shift Right Arithmetically (AQ) *	No	SRT
	Rotate Right (AQ) *	No	RTE
Branch	Branch and Store I	Yes	BSI
	Branch or Skip on Condition	Yes	BSC
	Modify Index and Skip * *	Yes	MDX
	Wait	No	WAIT
I/O	Execute I/O	Yes	XIO

* Letters in Parentheses Indicate Registers Involved in Shift Operations.
** If Long and not Indexed.

17151A

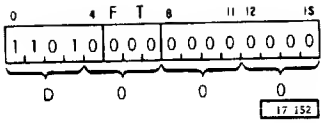


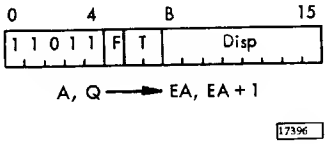
Figure 6. Hexadecimal Derivation

Hexadecimal Reprcsentation

The hexadecimal versions or version of each instruction is provided with its description. The hexadecimal number is derived by dividing the 16 bits of the instruction into groups of four bits and taking the binary-decimal value of each group. As shown in Figure 6, the hexadecimal number of the Store Accumulator instruction is D000 where D represents bit positions 0-3, and 000 represents bit positions 4-15 (no F, T, or displacement bits are assumed).

Instruction Format and Operation Symbology

Where possible, the following descriptions of 1800 P-C instructions include the instruction format with a symbolic summary of its operation. For example, the description of the Double Store instruction includes:

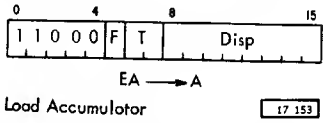


where the one word instruction format is provided with the op code 11011. The symbolic summary of the instruction (A, Q→EA, EA+1) is simply an attempt to illustrate that the contents of the accumulator (A) and its extension (Q) are stored at the effective address of the instruction (EA) and the next higher address (EA+1).

Symbols	Meaning
A, Q	Contents of accumulator and its extension
⟶	Are stored at
EA, EA+1	Effective address of the instruction and the next higher address.

LOAD AND STORE INSTRUCTIONS

$C000_{16}$ LOAD ACCUMULATOR (LD)

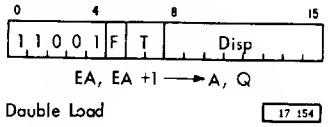


Description. The contents of the core storage location specified by the effective address (EA) of the instruction replace the contents of the Accumulator (A). The contents of the core storage location are unchanged.

Indicators. The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal. The hexadecimal version of the LD instruction is C000, assuming no F, T, or displacement bits.

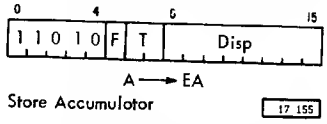
$C800_{16}$ DOUBLE LOAD (LDD)



Description. The contents of the core storage location specified by the instruction (EA) and the next higher core storage location are loaded into the Accumulator (A) and its extension (Q), respectively. This provides double precision load for use with the double precision arithmetic. The EA of the instruction must be an even address for correct operation. If the EA is odd, the contents of that location will be entered into both the Accumulator and its extension. The contents of core storage remain unchanged.

Indicators. The Carry and Overflow indicators are not changed by this instruction.

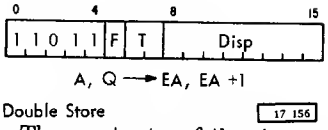
$D000_{16}$ STORE ACCUMULATOR (STO)



Description. The contents of the Accumulator replace the contents of the core storage location specified by the effective address. The contents of the Accumulator are unchanged.

Indicators. The Carry and Overflow indicators are not changed by this instruction.

$D800_{16}$ DOUBLE STORE (STD)



Description. The contents of the Accumulator (A) and its extension (Q) are stored at the core storage locations specified by the effective address (EA) and the EA+1. This provides double precision store for use with the double precision arithmetic. The EA of the instruction must be an even address for correct operation. If the EA is odd, the contents of the Accumulator are stored at the EA and the contents of the Accumulator Extension (Q) will not appear in core storage. The contents of A and Q remain unchanged.

Indicators. The Carry and Overflow indicators are not changed by this instruction.

6000_{16} LOAD INDEX (LDX)

Description. An Index Register (XR) or the Instruction Register (I) is loaded by the DISPLACEMENT, the ADDRESS, or the contents of the location specified by the ADDRESS. The T bits indicate which Register is loaded and the F and IA (2-word instruction only) bits determine the source of data.

As shown in Figure 7, if the F bit is 0 the register specified by T is loaded with the DISPLACEMENT. The eight high-order positions of the specified register is filled with the value of the sign bit (bit position 8 of instruction) to complete the 16-bit word.

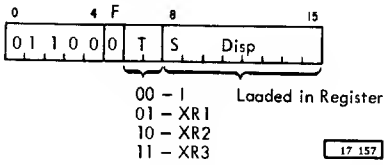


Figure 7. One-Word Load Index Instruction

If, however, the F bit is 1 (Figure 8), the loading of the register is dependent on the IA bit of the instruction. If the IA bit is 1, the register is loaded with the contents of the word specified by the ADDRESS; if 0, the register is loaded with the ADDRESS portion of the instruction

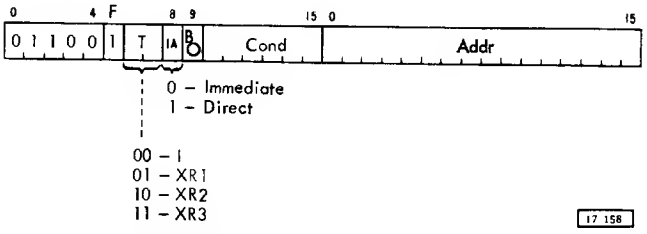


Figure 8. Two-Word Load Index Instruction

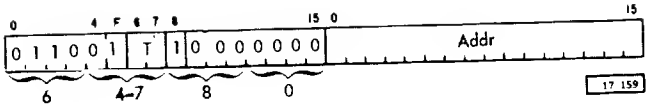


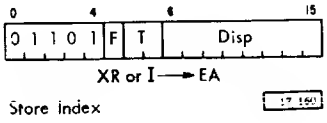
Figure 9. LDX Hexadecimal

Indicators. The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal. The hexadecimal versions of the LDX instruction depend on the F, T, and IA bits (Figure 9):

60xx	Load DISP into I (60xx-63xx are one word instructions and xx is the bit value of DISP)
61xx	Load DISP into XR1
62xx	Load DISP into XR2
63xx	Load DISP into XR3
6400	Load ADDRESS into I (6400-6700 and 6480-6780 are two word instructions)
6500	Load ADDRESS into XR1
6600	Load ADDRESS into XR2
6700	Load ADDRESS into XR3
6480	Load contents of word specified by ADDRESS into I
6580	Load contents of word specified by ADDRESS into XR1
6680	Load contents of word specified by ADDRESS into XR2
6780	Load contents of word specified by ADDRESS into XR3

6800_{16} STORE INDEX (STX)



Description. An Index Register, or the Instruction Register, will be stored in core storage at the Effective Address (EA). The T bits specify which register will be stored and bits 5 (F bit) and 8 (IA) will govern the generation of the Effective Address.

T = 00	I Register
T = 01	XR1
T = 10	XR2
T = 11	XR3
F = 0	EA = I register + DISPLACEMENT
F = 1	Bit 8 = 0 (IA bit): EA = Location specified by address portion of the instruction.
F = 1	Bit 8 = 1 (IA bit): EA = Address located in the word specified by the address portion of the instruction.

Indicators. The Carry and Overflow indicators are not affected.

Hexadecimal. The hexadecimal versions of the STX instruction depend on the F, T, and IA bits (Figure 10):

68xx	I is stored at EA	EA = I + DISP (xx is value of DISP)
69xx	XR1 is stored at EA	
6Axx	XR2 is stored at EA	
6Bxx	XR3 stored at EA	
6C00	I stored at EA	EA = ADDRESS
6D00	XR1 stored at EA	
6E00	XR2 stored at EA	
6F00	XR3 stored at EA	
6C80	I stored at EA	EA = Contents of word specified by ADDRESS
6D80	XR1 stored at EA	
6E80	XR2 stored at EA	
6F80	XR3 stored at EA	

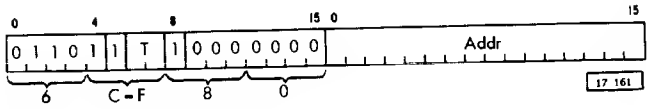


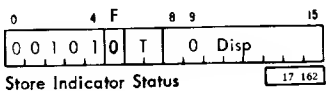
Figure 10. STX Hexadecimal

STORE STATUS (STS)

Description. Depending on bit 9, the Store Status instruction is used in either of two operations:

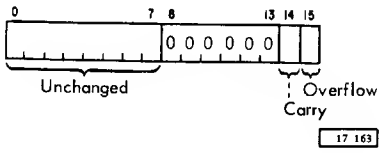
1. Store the status of the Carry and Overflow indicators.
2. Write or clear the storage protect bit from the core storage address specified by the instruction.

2800_{16} Store Status



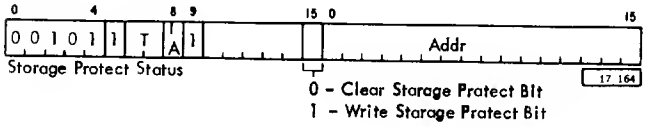
Bit 9 must equal zero. The conditions of the Carry and Overflow indicators are stored in the low-order bits of the word specified by the effective address: Carry indicator at bit 14 and the Overflow indicator at bit 15.

Bits 0 through 7 of the word remain unchanged and bits 8 through 13 will be reset to zero. The indicators will be reset. An ON status will store a one bit; and an OFF status a zero bit.



Indicators. The Carry and Overflow indicators are reset as they are stored.

$2C40_{16}$ or $2C41_{16}$ Write or Clear Storage Protect Bit

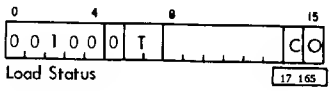


Bit 9 must equal 1. A two word instruction (F bit equals 1) must be used. Bit 15 determines whether the storage protect bit for the word specified by the effective address of the instruction is written or cleared:

B15 is zero -- Storage protect bit is cleared.
B15 is one -- Storage protect bit is written.

However, the Write Storage Protection Bit switch on the P-C console must be on to write storage protection bits. The program continues to have the ability to write or clear storage protection bits as long as this switch remains in the on position.

2001_{16} LOAD STATUS (LDS)



Description. This instruction applies to the single word format only. The Carry and Overflow indicators will be loaded with the status of the bits in positions 14 (Carry) and 15 (Overflow) of the instruction. Normally this status was stored into this instruction by a previous Store Status instruction. Memory will remain unchanged. A one bit will cause an indicator ON condition and a zero bit an indicator OFF condition.

Indicators. The Carry and Overflow indicators are set according to the bits at positions 14 and 15.

Hexadecimal. The hexadecimal version of this instruction is 200x (assuming no F and T bits, and zero bits in positions 8-11). The units hexadecimal integer depends on how the indicators are to be set (Figure 11).

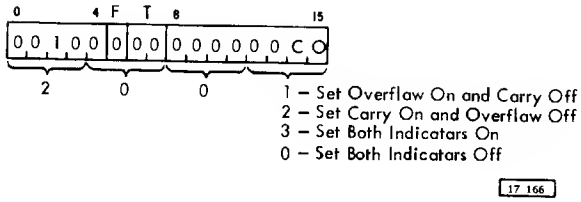
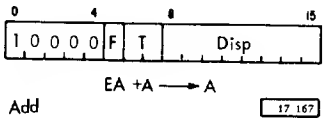


Figure 11. LDS Hexadecimal

ARITHMETIC INSTRUCTIONS

8000_{16} ADD(A)

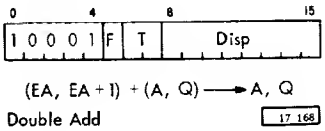


Description. The contents of the memory location specified by the instruction are added to the contents of the accumulator. The result replaces the contents of the accumulator. Two's complement arithmetic is used; that is, negative operands and/or sums will be in two's complement form. The contents of memory remain unchanged. See Appendix C for details of "data addition."

Indicators. The Overflow indicator will be turned ON if the magnitude of the sum is too large to be represented in the Accumulator; that is, greater than $+2^{15}-1$ or less than -2^{15}. This is detected by a resultant carry or borrow out of only one of the two high-order bit positions of the accumulator. If Overflow was previously ON, it will not be changed. Overflow can be reset by testing, or a Load or Store

Status instruction. See Branch or Skip on Condition instruction. The Carry indicator will be set by a carry out of the high-order bit position of the accumulator.

8800_{16} DOUBLE ADD (AD)



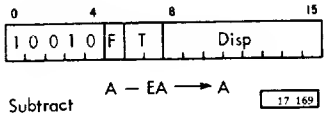
Description. The contents of the core storage location specified by the instruction and the next higher addressed location are added to the contents of the Accumulator (A) and its extension (Q). This provides double precision addition where the Accumulator and its extension are considered as one 32 bit accumulator. The sum replaces the contents of A and Q. Core Storage remains unchanged.

The effective address formed by the instruction must be an even address for correct operation. If the effective address is odd, the contents of that location is added to both the Accumulator and its extension.

Indicators. When the instruction is completed, the Carry indicator represents the results of this instruction — not previous instructions. The Carry indicator is set ON by detection of a Carry out of the high-order position of the Accumulator.

The Overflow indicator will be turned ON by this instruction if the magnitude of the sum is greater than $+2^{31}-1$ or less than -2^{31}. If this indicator was ON before the instruction, no change will occur. If OFF, it will be turned ON when the magnitude of the number is too large to be represented. This is detected by a carry out of only one of the two high-order bits of the Accumulator.

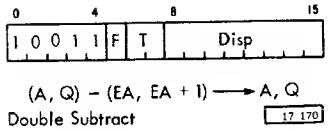
9000_{16} SUBTRACT (S)



Description. The contents of the core storage location specified by the instruction are subtracted from the contents of the Accumulator. The result replaces the contents of the Accumulator. Two's complement arithmetic is used; that is, both negative operands and differences will be in two's complement form. Core Storage remains unchanged.

Indicators. The Overflow indicator will be turned ON if the magnitude of the difference is too large to be represented in the Accumulator; that is, greater than $+2^{15}-1$ or less than -2^{15}. If Overflow was previously ON, it will not be changed. (Overflow can be reset by testing or a Load or Store Status instruction. See Branch or Skip on Condition Instruction.) This is detected by a borrow from only one of the two high-order bit positions of the accumulator. The Carry indicator will be set by a borrow from the high-order position.

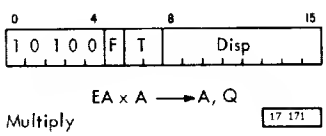
9800_{16} DOUBLE SUBTRACT (SD)



Description. The contents of the core storage location specified by the instruction and the next higher memory location are subtracted arithmetically from the contents of the Accumulator (A) and its extension (Q). This provides double precision subtraction where the Accumulator and its extension are considered as one 32-bit accumulator. The difference replaces the contents of A and Q. Memory remains unchanged. The effective address formed by the instruction must be an even address for correct operation. If the effective address is odd, the contents of that location are subtracted from both the Accumulator and its extension.

Indicators. The Overflow indicator will be turned ON if the magnitude of the difference is too large to be represented in the Accumulator (A) and its extension (Q), or more specifically, greater than $+2^{31}-1$ or less than -2^{31}. This is detected by a borrow from only one of the two high-order bit positions of the Accumulator. If Overflow was previously ON, it will not be changed. (Overflow can be reset by testing or by a Load or Store Status instruction. See Branch or Skip on Condition instruction.) The Carry indicator will be set by a borrow from the high-order position.

$A000_{16}$ MULTIPLY (M)

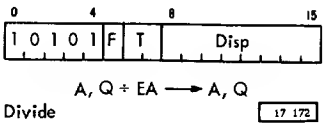


Description. The content of the core storage location specified by the instruction (multiplicand) is multiplied algebraically by the content of the Accumulator (multiplier). The 32-bit product replaces the content of the Accumulator (A) and its extension (Q). The most significant bits of the product are in the Accumulator. Core storage remains unchanged. The product is in the double precision format.

Indicators. Neither the Overflow nor the Carry indicators are changed.

Programming Note. The largest product that can be developed is 2^{30}. This occurs when the multiplier and multiplicand are both the largest negative numbers, -2^{15}.

$A800_{16}$ DIVIDE (D)

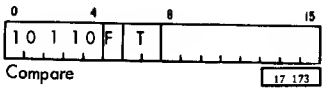


Description. The content of the Accumulator and its extension (a 32-bit double precision word) is divided by the content of the core storage location specified by the instruction. The quotient and remainder replace the contents of the Accumulator and the Accumulator extension, respectively. The "sign" of the remainder will be the same as the dividend.

The largest dividend that can correctly be operated upon is $2^{30} + 2^{15}-1$ if divided by the largest positive or negative divisor.

Indicators. The Overflow indicator will be turned ON when division by zero is attempted or when the quotient overflow condition exists. A quotient overflow occurs when the factors are such that the quotient would exceed the range of -2^{15} to $+2^{15}-1$. An overflow will cause the Accumulator and its extension (Q) to be left in an undefined state.

$B000_{16}$ COMPARE (CMP)



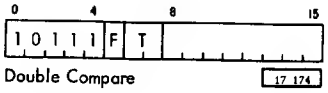
Description. The content of the Accumulator (A) is algebraically compared against the content of the word at the effective address, and the Instruction Register (I) is modified according to the result of the comparison as shown below:

if A > C(EA) then I = I
if A < C(EA) then I = I + 1
if A = C(EA) then I = I + 2

The contents of A and Q and core storage will be unchanged at the end of the instruction execution.

Indicators. The Overflow indicator is unaffected by this instruction. The Carry indicator may be altered.

$B800_{16}$ DOUBLE COMPARE (DCM)



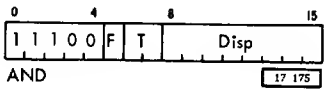
Description. The contents of the Accumulator (A) and its Extension (Q) are compared against the contents of the effective address (even) and the effective address plus one (odd). The Instruction Register (I) is modified as follows:

if A, Q > C(EA), C(EA + 1), then I = I
if A, Q < C(EA), C(EA + 1), then I = I + 1
if A, Q = C(EA), C(EA + 1), then I = I + 2

If the EA is odd, the contents of that location are compared against the contents of both A and Q. The contents of A and Q and core storage will be unchanged at the end of the instruction executions.

Indicators. The Overflow indicator is unaffected by this instruction. The Carry indicator may be altered.

$E000_{16}$ LOGICAL AND (AND)



Description. The contents of the core storage location specified by the instruction are ANDed bit by bit with the contents of the Accumulator. The following table defines the AND operation.

AND

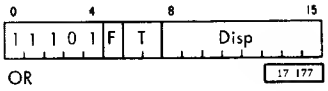
Memory	1	1	0	0
Accum	1	0	1	0
Result	1	0	0	0

17 176

The result replaces the contents of the Accumulator. Core storage remains unchanged.

Indicators. The Carry and Overflow indicators are not changed by this operation.

$E800_{16}$ LOGICAL OR (OR)



Description. The contents of the core storage location specified by the instruction are ORed bit by bit with the contents of the Accumulator. The following table defines the OR operation:

OR

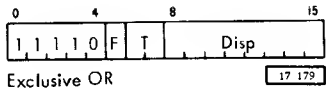
Memory	1	1	0	0
Accum	1	0	1	0
Result	1	1	1	0

17 178

The result replaces the contents of the accumulator. Core storage remains unchanged.

Indicators. The Carry and Overflow indicators are not changed by this operation.

$F000_{16}$ LOGICAL EXCLUSIVE OR (EOR)



Description. The contents of the core storage location specified by the instruction are Exclusive ORed bit by bit with the contents of the Accumulator. The following table defines the Exclusive OR operation:

Exclusive OR

Memory	1	1	0	0
Accum	1	0	1	0
Result	0	1	1	0

17 180

The result replaces the contents of the Accumulator. Core storage remains unchanged.

Indicators. The Carry and Overflow indicators are not changed by this operation.

SHIFT INSTRUCTIONS

All shift instructions are single word format only (F = 0). They are divided into subclasses as defined by bit positions 8 and 9. Those that have their shift count defined by the TAG bits will shift as shown in Table 3.

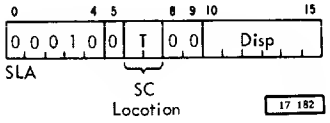
Table 3. Shift Count

Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3

17 181

If the shift count is zero, the instruction will perform as a No-OP.

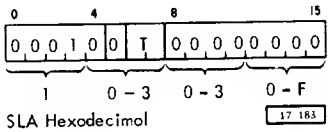
1000_{16} SHIFT LEFT LOGICAL A (SLA)



Description. The Accumulator (A) will be shifted left the number of spaces specified by the Shift Count (Table 4). Vacated bit positions will be set to zero. Bits leaving the high-order (bit 0 of A) position are shifted into the Carry indicator (see Indicators below). The Extension (Q) is not affected. Note that bit positions 8 and 9 must be 00.

Indicators. The Carry indicator is turned on and off for each one or zero shifted left from the high-order position of A. The Overflow indicator is unaffected.

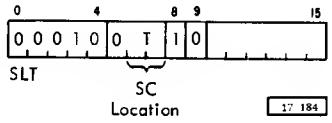
Hexadecimal. The hexadecimal versions of the SLA instruction depend on the TAG bits.



10XX	Shift count in displacement
1100	Shift count in XR1
1200	Shift count in XR2
1300	Shift count in XR3

The XX in 10XX (above) is the unknown value of the 6 low-order bits of the DISPLACEMENT when the TAG bits are 00.

1080_{16} SHIFT LEFT LOGICAL A & Q (SLT)

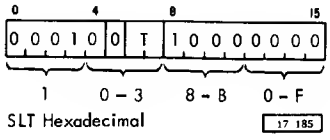


Description. The Accumulator (A) and its extension (Q) are shifted left as a 32-bit double precision register. Vacated bit positions will be set to zero. Bits leaving the high-order position (bit position 0 of A) are shifted into the Carry indicator.

Indicators. The Carry indicator is turned on and off for each one or zero shifted left from high-order position of A. The Overflow indicator is unaffected.

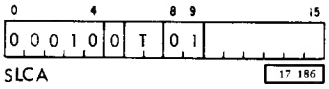
Hexadecimal. The hexadecimal versions of this instruction depend on the TAG bits.

*108X	Shift count is displacement
1180	Shift count in XR1
1280	Shift count in XR2
1380	Shift count in XR3



*The second low-order integer of 108X can actually be any integer from 8 through B, depending on the unknown bit values in positions 10 and 11. The unknown values of bit positions 12-15 are represented by X.

1040_{16} SHIFT LEFT AND COUNT A (SLCA)



Description. A TAG of 00 causes this instruction to be performed as a Shift Left A instruction. A TAG specifying one of the index registers causes the shift count to be transferred from the low-order six bits of the specified register to the shift counter. This count will be decremented by one for each position that the contents of the Accumulator (A) are shifted to the left. Vacated bit positions are set to zero.

The shift terminates when either a "1" is shifted into the high-order position of A (the "1" remains in the high-order position after the instruction has terminated) or the shift count has been decremented to zero. The decremented count is then loaded back into the six low-order bit positions of the index register and bits 8 and 9 are reset to zero. Bit positions 0-7 of the index register remain unchanged at completion of the instruction.

Indicators. The Carry indicator will be OFF if the shift is terminated by the detection of the count reaching zero. The Carry indicator will be ON if the shift is terminated by the detection of a 1 in the A0 position before the shift count reaches zero.

For T = 0 the Carry indicator is set as in Shift Left instruction. The Overflow indicator is unaffected.

Hexadecimal. The hexadecimal versions of this instruction depend on the TAG bits.

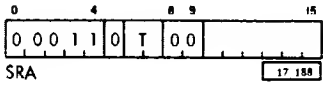
104X	Shift Left A
1140	Shift Count in XR1
1240	Shift Count in XR2
1340	Shift Count in XR3

$10C0_{16}$ SHIFT LEFT AND COUNT A & Q (SLC)

Description. This instruction is the same as the Shift Left and Count A except that both the Accumulator (A) and its Extension (Q) are shifted. Bit positio 0 of Q is shifted into bit position 15 of A and vacated positions at the right of Q are set to zero.

Hexadecimal. The hexadecimal versions of the SLC instruction are 10XX, (the second integer must be C-F), 11C0, 12C0, and 13C0.

1800_{16} SHIFT RIGHT LOGICAL A (SRA)

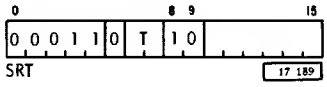


Description. The Accumulator (A) is shifted right the number of places indicated by the Shift Count. Zeros are entered in all vacated spaces. The Extension (Q) is undisturbed. Low-order bits of A are lost.

Indicators. The Carry and Overflow indicators are not changed.

Hexadecimal. 180X, 1900, 1A00, 1B00

1800_{16} SHIFT RIGHT A & Q (SRT)



Description. The Accumulator (A) and Extension (Q) are shifted right as a 32-bit double precision register. The value of the Sign (bit position 0 of A) is entered in all vacated spaces. Low-order bits of Q are lost.

Indicators. The Carry and Overflow indicators are not changed.

Hexadecimal. 188X, 1980, 1A80, 1B80

$18C0_{16}$ ROTATE RIGHT A & Q (RTE)

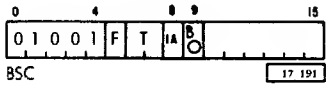
Description. The Accumulator (A) and Extension (Q) are rotated to the right as a 32-bit double precision register the number of bit positions specified by the Shift Count. Bit position 15 of the Extension (Q) is linked to bit position 0 of the Accumulator (A) to form a continuous loop so that the high-order positions of the Accumulator pick up the bits dropped from the low-order positions of the Extension.

Indicators. The Carry and Overflow indicators are not changed.

Hexadecimal. 18XX (The second integer is C-F), 19C0, 1AC0, 1BC0.

BRANCH INSTRUCTIONS

$48XX_{16}$ BRANCH OR SKIP ON CONDITION (BSC)



Description. There are six testable conditions associated with the Accumulator. These conditions may be tested by indicating the bit pattern in the DISPLACEMENT of the instruction.

The six Accumulator conditions that can be tested are shown by bit position.

Bit	Condition
15	Overflow OFF
14	Carry OFF
13	Accumulator Even
12	Accumulator Plus (greater than zero)
11	Accumulator Negative
10	Accumulator Zero

When F = 0, the instruction executed is a Skip on Condition when one or more of the conditions specified is true. This enables the program to skip over the next one word instruction. If none of the conditions specified are true, the next instruction in sequence is executed.

When F = 1, the instruction executed is a Branch to the Effective Address (EA) when none of the condition(s) specified are true. If any one of the condition(s) specified in bit positions 10-15 is true, the next instruction in sequence is executed. Examples are shown in Figure 12.

The EA is calculated as follows:

F = 1	IA = 0	T = 00	EA = ADDR
		T = 01	EA = XR1 + ADDR
		T = 10	EA = XR2 + ADDR
		T = 11	EA = XR3 + ADDR

When the IA bit is equal to a one (IA = 1), this instruction enables the program to return to a main-line program from a program subroutine or interrupt routine. This is accomplished by making the

Bit Positions:	10	11	12	13	Skip	Bronch
ACC Conditions:	Zero	Minus	Plus	Even	(F = 0)	(F=1)
Test Conditions	1	1	1	0	Alwoys	Never
	0	0	0	0	Never	Alwoys
	0	0	1	0	Plus	Not Plus
	1	1	0	0	Not Plus	Plus
	0	1	0	0	Minus	Not Minus
	1	0	1	0	Not Minus	Minus
	1	0	0	0	Zero	Not Zero
	0	1	1	0	Not Zero	Zero
	0	0	0	1	Even	Odd
	0	0	1	1	Even or Plus	Odd ond Minus
	0	1	0	1	Even or Minus	Odd ond Plus

Notes: 1. ACC plus ond minus ore non zero conditions.
2. Skip ond Bronch columns specify action or ACC condition required for Skip or Bronch.

17441

Figure 12. BSC Examples

EA of this instruction identical to the EA of a previously executed Branch and Store Instruction Register (BSI) instruction. The EA as calculated below is loaded into the Instruction Register.

F = 1 IA = 1	T = 00	EA = *C(ADDR)
	T = 01	EA = C(XR1 + ADDR)
	T = 10	EA = C(XR2 + ADDR)
	T = 11	EA = C(XR3 + ADDR)

*C means "Contents of"

Programming Note. When an interrupt request has been detected by a priority level, the program is directed to service the request by interrupting. During the servicing, all interrupt requests of equal or lower status are effectively constrained from interrupting while the servicing of the higher priority is in progress. However, if a request is detected for a higher priority level than is presently in progress, the program is immediately interrupted again. This is frequently called Nesting of Interrupts.

At the completion of servicing any level of interrupt, it is necessary to signal the priority hardware to reset the priority-status of the highest level that is on. This reset permits lower priority requests that may have been temporarily constrained but recorded to be accepted once again by the P-C. This is effected by making Bit 9 = 1 in this instruction. This programmed recognition of waiting interrupts should not be confused with a normal subroutine linkage back to a mainline program in which Bit 9 should be set to zero.

The BSC is a conditional instruction. When Bit 9 = 1, the reset of the interrupt level occurs when the Branch or Skip occurs. If the Branch or Skip does not occur, the interrupt level is not reset.

Indicators. The Overflow indicator will be reset when testing. The Carry indicator is not reset by testing. The contents of the Accumulator are not changed by testing. If no conditions are specified, a Skip will not occur on the SKIP instruction (F = 0) or a branch will occur on the BRANCH instruction (F = 1).

Hexadecimal. The hexadecimal versions of the BSC instruction depend on the F, T, IA, B0 and condition bits.

48XX	Skip on any condition
4C0X	Branch to ADDR on no condition
4D0X	Branch to XR1 + ADDR on no condition
4E0X	Branch to XR2 + ADDR on no condition
4F0X	Branch to XR3 + ADDR on no condition

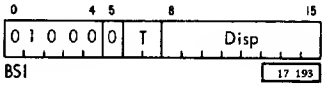
The second lower-order digit for the four instructions above (4C0X - 4F0X) may actually be any digit from 0 to 7.

4C8X	Branch to contents of ADDR on no condition
4D8X	Branch to contents of XR1 + ADDR on no condition
4E8X	Branch to contents of XR2 + ADDR on no condition
4F8X	Branch to contents of XR3 + ADDR on no condition

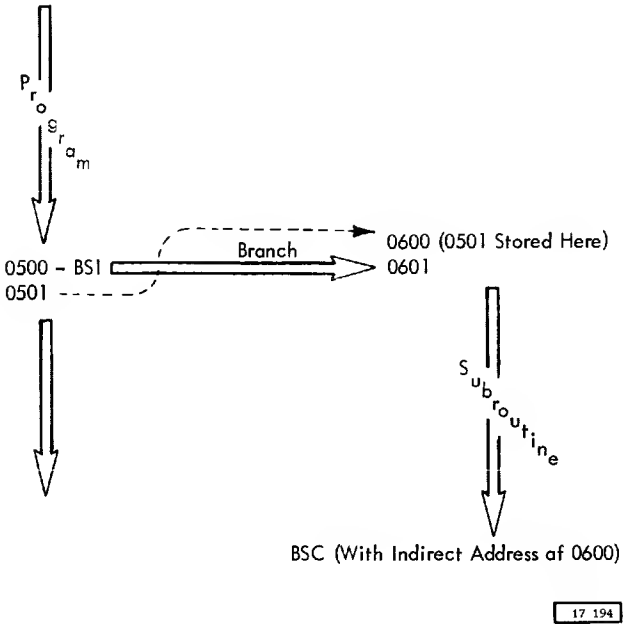
The second integer for the four instructions above may actually be any integer from 8 through F.

4000_{16} BRANCH AND STORE INSTRUCTION REGISTER (BSI)

Description. When F = 0 (one word format), the contents of the Instruction Register are stored in the core storage location specified by the effective address. The stored address is that of the next instruction in the normal sequence. The Instruction Register is then set to the value of the effective address plus one, and program execution proceeds from that point.



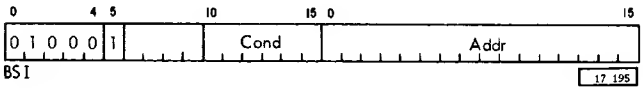
For example, a BSI instruction located at core storage address 0500, with an effective address of 0600, would store the address 0501 at location 0600 and then branch to 0601.



A BSC instruction with an IA bit of one and an ADDRESS of 0600 would be used to return from the subroutine.

When F = 1 (two word instruction format), the above function is conditionally executed depending on the condition bits specified in the Displacement. These Accumulator condition bits are defined in the preceding BSC instruction. If any one of the conditions specified is true, the previously explained branch does not occur. Instead, the next instruction in sequence is preformed. If none of the conditions are true, the Instruction Register is stored at the effective address (specified by the ADDRESS) and the branch is to EA + 1.

Interrupts are suppressed for the first instruction following a BSI instruction or an interrupt. Therefore, the Mask Register (see Interrupt section) may be set without the possibility of an interrupt immediately following the BSI instruction or the interrupt.



Indicators. When F = 0, the status of the indicators is unchanged. When F = 1, the Overflow indicator is reset if tested.

Hexadecimal. The hexadecimal versions of the BSI instruction depend on the F and condition bits:

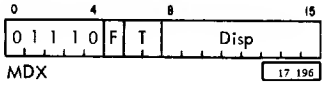
40XX	Branch to EA + 1 (I stored at EA)
44XX	Branch to EA + 1 on no condition. (I stored at EA)

7000_{16} MODIFY INDEX AND SKIP (MDX)

Description. The Modify Index and Skip has many uses. Either an Index Register, the Instruction Register, or a word in core storage can be modified by a value specified by the instruction. This value depends on the instruction format and may be the Displacement, the Address, or the contents of the Address. The specific operation and register involved depends upon the instruction format as described below.

The Instruction Register is incremented an additional time to cause a skip whenever a modified Index Register or core storage word is at zero when the operation is complete, or changed sign during the operation.

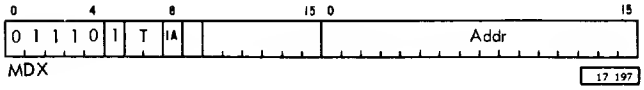
One Word Instruction Form (F bit = 0)



The DISP is added to the Instruction Register or an Index Register, depending on the TAG bits:

T = 00	DISP is added to I If DISP = 0, this is a NO-OP. If DISP = 1, this is a skip. If DISP > 1, this is an unconditional branch.
T = 01	DISP is added to XR1
T = 10	DISP is added to XR2
T = 11	DISP is added to XR3

Two Word Instruction Format (F bit = 1)



If the TAG bits are 00, the DISP (bits 8 through 15 of the first word) is added to the contents of the core storage location specified by the ADDRESS. (This is an Add to Memory.) The Accumulator is not changed.

If the TAG bits are other than 00, bit position 8 is the controlling factor:

Bit 8 = 0

T = 01 ADDRESS is added to XR1
T = 10 ADDRESS is added to XR2
T = 11 ADDRESS is added to XR3

Bit 8 = 1

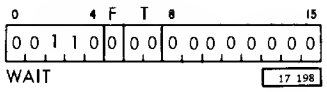
T = 01 Contents of word specified by Address is added to XR1
T = 10 Contents of word specified by Address is added to XR2
T = 11 Contents of word specified by Address is added to XR3
(The Address specified above being the location provided by the ADDRESS of the instruction.)

Indicators. The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal. The hexadecimal versions of the MDX instruction depend on the F, T, and displacement bits.

70XX	Add DISP to I
71XX	Add DISP to XR1
72XX	Add DISP to XR2
73XX	Add DISP to XR3
74XX	Add DISP to contents of ADDR
7500	Add ADDR to XR1
7600	Add ADDR to XR2
7700	Add ADDR to XR3
7580	Add contents of word specified by ADDR to XR1
7680	Add contents of word specified by ADDR to XR2
7780	Add contents of word specified by ADDR to XR3

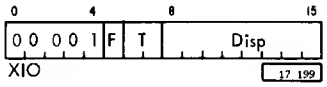
3000_{16} WAIT (WAIT)



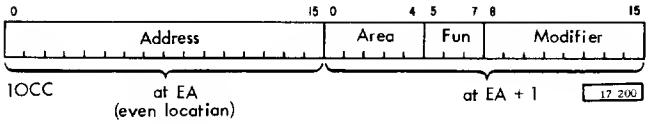
Description. This instruction is a one word format instruction only. The P-C stops in a wait condition. It can be restarted manually or by detection of an interrupt. Following completion of an interrupt subroutine, the instruction immediately following the Wait instruction will be executed if the Branch Out of Interrupt is indirect. Data Channel operations will continue during the Wait condition.

Indicators. The Carry and Overflow indicators are not changed by this instruction.

0800_{16} EXECUTE I/O (XIO)



Description. This instruction is used for all I/O operations; it may be either one or two words in length, as specified by the F-bit. In the two-word instruction, the Address is either a direct or indirect address, as specified by the IA bit. For proper operation, the Effective Address must be an even address. The Effective Address is used to select a two-word I/O Control Command (IOCC) from storage. The IOCC specifies the I/O operation, I/O device, and core storage address. The format of the two-word IOCC follows, with an explanation of the assigned fields:



Area

This 5-bit field specifies a unique segment of I/O which may be a single device (1442 Card Read Punch, 1443 Printer, etc.) or a group of several units (magnetic tape drives, serial I/O units, contact sense units, etc.). (See Appendix D.)

Area 00000 is used to address such devices as the Console and the Interrupt Mask Register. (See Area Code Zero following XIO Data Flow.)

Function

The primary I/O functions are specified by the 3-bit function code of the IOCC:

000 - This code is used to remove an I/O device from on-line status and place it in CE mode. It can also be used to restore the on-line status and remove the CE mode.

001 - Write
This code is used to transfer a single word from storage to an I/O Unit. The

address of the storage location is provided by the Address field of the I/O Control Command.

010 - Read
This code is used to transfer a single word from an I/O unit to storage. The address of the storage location is provided by the Address field of the I/O Control Command.

011 - Sense Interrupt Level
This code directs the I/O devices requesting interrupt recognition to make their status available in the Accumulator as the Interrupt Level Status word (see Interrupt section).

100 - Control
This code causes the selected device to interpret the Address word of the IOCC as a specific control action. (See Area Code Zero following XIO Data Flow.)

101 - Initialize Write
This code initiates a WRITE operation on a device or unit which will subsequently make data transfers from storage via a Data Channel.

110 - Initialize Read
This code initiates a READ operation from a device or unit which will subsequently make data transfers to storage via a Data Channel.

111 - Sense Device
This code causes the selected device to make its current status available in the Accumulator as the Device Status Word.

If Area 00000 is specified, the Console status or Interval Timer status may be brought into the Accumulator as specified by a unit address code in the Modifier field.

Programming Note:

The current content of the Accumulator is destroyed by the execution of Sense Interrupt Level, Sense Device, Initialize Read, Initialize Write, Read, and Write. Therefore, it is the programmer's responsibility to save the Accumulator content, if necessary.

Modifier

This 8-bit field provides additional detail for either Function or Area. For example, if the Area specifies a Disk Storage Drive, and if the Function specifies Control (100) then a particular modifier code specifies the Seek operation. In this case, the Modifier serves to extend the Function.

If, however, the Area specifies a group of Serial I/O devices, and if the Function specifies Write (001), then the particular unit address is specified by the Modifier. (See Appendix D.)

Address

The meaning prescribed for this 16-bit field is dependent upon the Function specified by this I/O control Command:

1. If Function = Initialize Write (101) or if Function = Initialize Read (110), then Address specifies the starting address of a table in storage (an I/O block). The contents of this table are data words and control information.
2. If Function = Control (100) and if, for example, Area specifies a 1443 Printer, the Address may specify a specific control action.
3. If Function = Sense (011) or (111), the Address field is ignored. Instead, an increment of time equivalent to a memory cycle is taken, during which the selected I/O device or Interrupt Level places its status word in the Accumulator.
4. If Function = Write (001) or if Function = Read (010), then Address specifies storage location of the data word.

Hexadecimal. The hexadecimal version of the XIO instruction is 08XX. The third integer may be any integer between 8 and F, depending on the F and T bits.

XIO Execution Data Flow

The circled numbers in Figure 13 correlate with the data flow sequence that follows:

1. The EA of the XIO is developed in the Accumulator (A) and routed to the Storage Address Register (SAR) to locate the IOCC.
2. Bit position 15 of SAR is forced on to select the EA + 1 where the IOCC Area, Function, and Modifier are found.

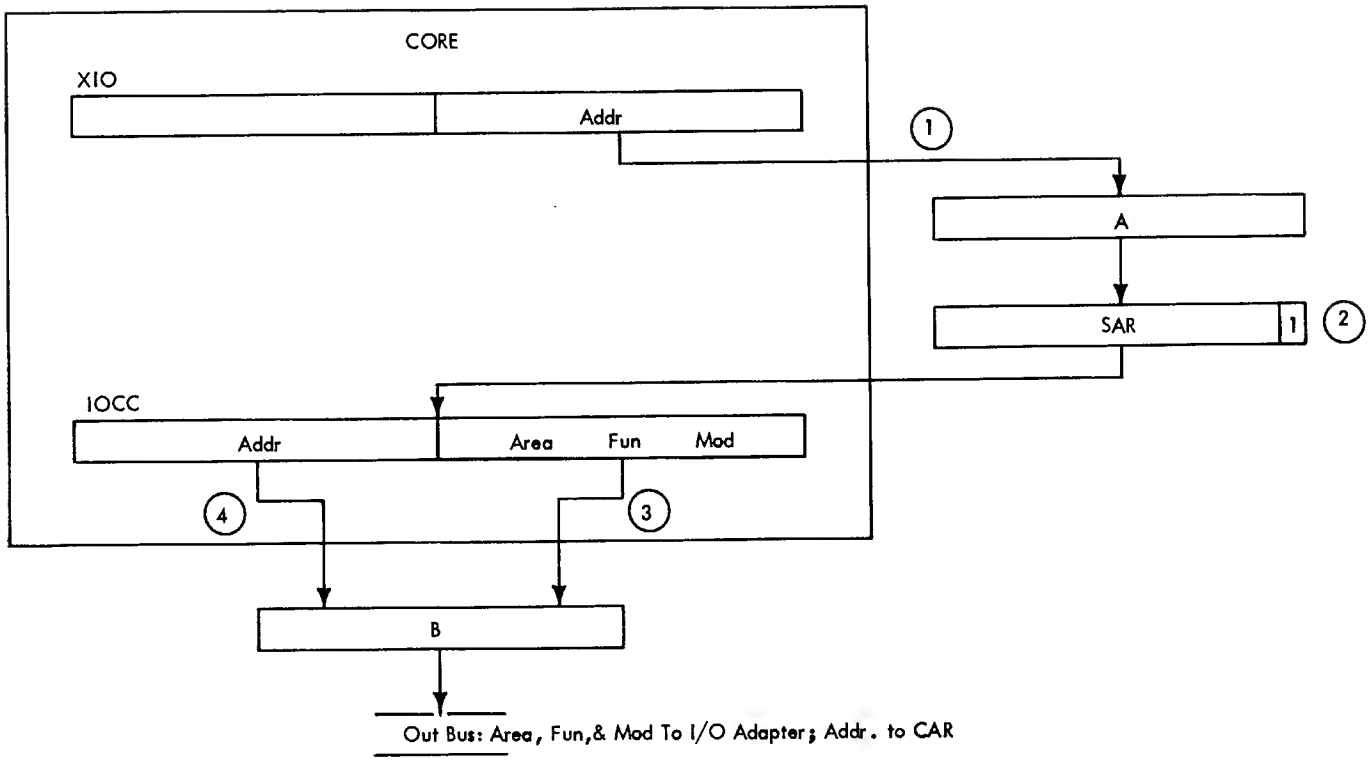


Figure 13. XIO Data Flow

3. The Area, Function, and Modifier are routed through the B-register to the Out-Bus to the I/O Adapter of the device specified by the Area.
4. If the Function is an Initialize Read/Write or Control, the Address part of the IOCC is routed through the B-register to the Out-Bus. The address part of the Initialize Read/Write IOCC's goes to the Channel Address Register (CAR) of the Data Channel. If the Function is Read or Write, the Address is routed through the A-register to the SAR. SAR addresses the storage location to or from which data is transmitted.

AREA CODE ZERO

The IOCC Area code 00000 is used with Modifier bits 8-10 to specify the particular feature or register listed below. These bits are fixed for all 1800 systems:

Feature/Register	Bits 8-10
Interval Timers	001
Console Data Entry Switches	010
Console Sense and Program Select Switches, and CE Switches	011
Interrupt Mask Register	100
Programmed Interrupt	101
Console Interrupt	110
Operations Monitor	111

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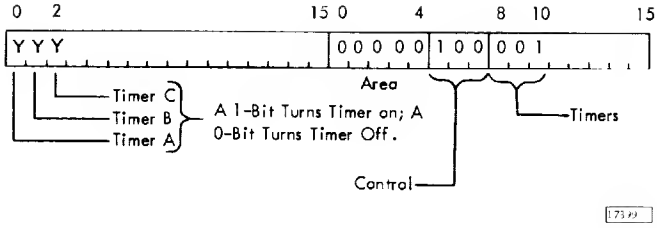
The IOCC for each operation follows. Note that the Function specifies the operation. Those bit positions left blank are not used.

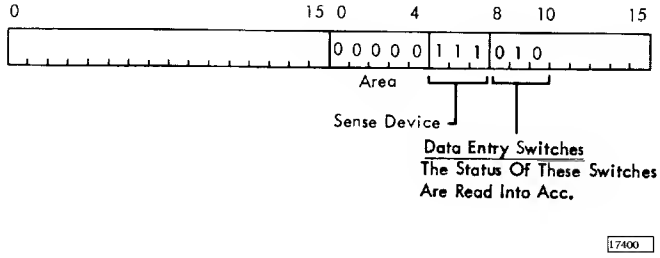
Interval Timers

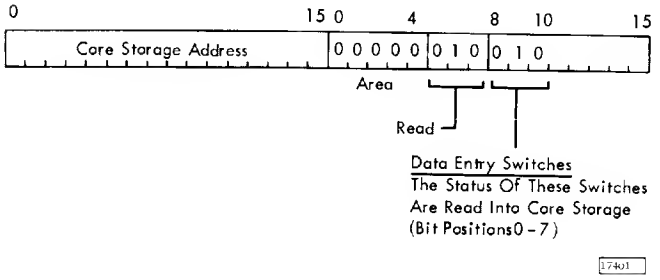
This IOCC is used to start or stop the interval timers. See Interval Timers section.

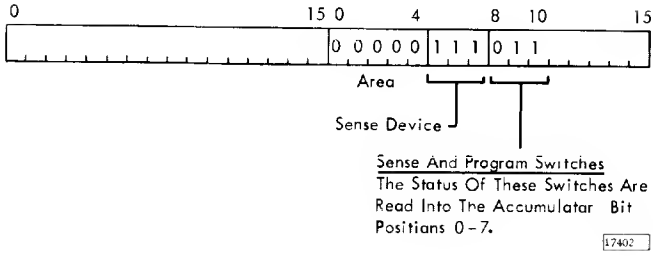


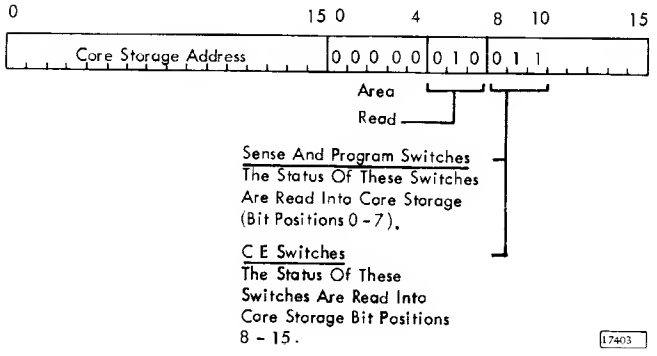
Console Data Entry Switches
Console Sense and Program Switches

The following IOCC's are used to read the console switches into the accumulator or core storage.



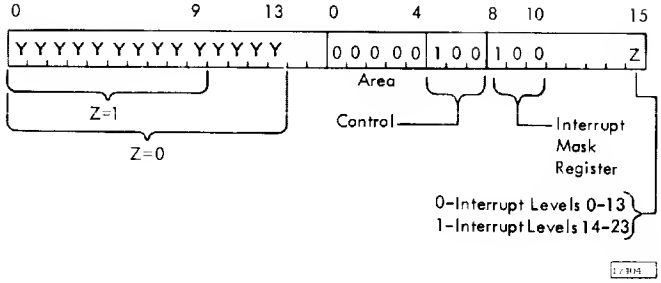






Interrupt Mask Register

This IOCC is used to mask or unmask customer interrupt levels 0-23.



Y - The status of bit positions 0-13 or 0-9, depending on Z, are copied into bit positions 0-13 or 14-23 of the 24-bit Interrupt Mask register.

A 1-bit turns the corresponding Mask register bit on. This prevents the interrupt on that particular level from being acknowledged until the mask is changed to unmask.

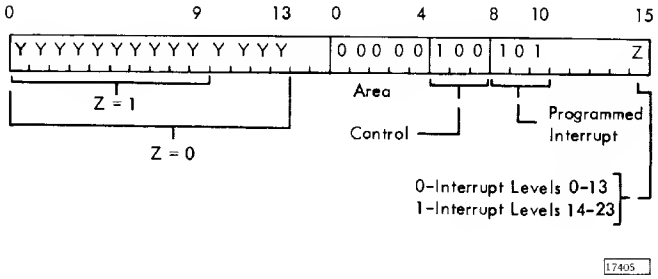
A 0-bit causes the Mask register bit to be set off, which enables the particular interrupt level.

The execution of this instruction does not destroy the contents of the accumulator.

NOTE: Pressing the Console Reset key masks interrupt levels 0-23.

Programmed Interrupt

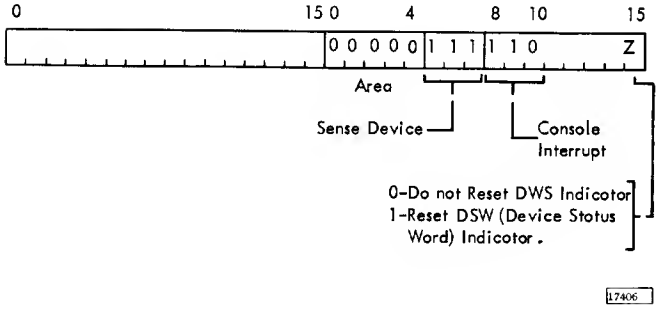
This IOCC is used to initiate an interrupt (or interrupts) from within the program. Programmed interrupts do not turn on bits in the ILSW.



Y - A 1-bit in positions 0-13 or 0-9, depending on Z, turns on corresponding interrupt level 0-13 or 14-23.

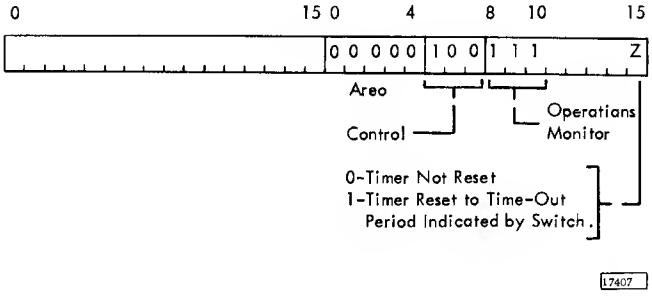
Console Interrupt

This IOCC is used to read the Console Interrupt Device Status Word (DSW) into the accumulator.



Operations Monitor

This IOCC is normally used to reset the Operations Monitor timer, thereby preventing time-out and the resulting alarm that would otherwise occur.



INTERVAL TIMERS

Three timers are provided to supply real-time information to the program. They are in core storage locations 0004 (timer A), 0005 (timer B), and 0006 (timer C). Each timer has a permanent time base which can be selected by the customer (Table 4). All three timers can operate at different time periods.

Table 4. Interval Timers

Core Storage Cycle Times	Available Time Bases (In Milliseconds)									
2 μsec	.125	.25	.5	1	2	4	8	16	32	64
4 μsec	.25	.5	1	2	4	8	16	32	64	128

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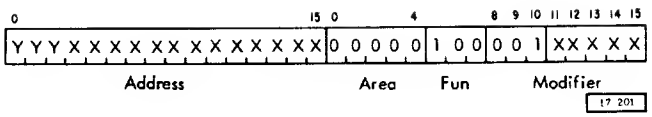
The timers can be started or stopped under program control. Once started, they are automatically incremented one count at a time through the cycle stealing facility of the P-C. A count is added each time the assigned time base period is completed. This count is automatic and does not require a program. The count of the timers proceeds in the positive direction. When the count reaches the largest positive value ($2^{15}-1$), the count continues to the most negative value and then through the negative numbers (two's complement) toward zero. When the count reaches zero, an interrupt is requested on the level assigned to the timers. (All three timers are on the same interrupt level which is assigned by the user.) The timer continues to operate after the zero value has been reached.

The timers, once operating, continue to record time correctly when the P-C is in the Run, Trace, or SI W/CS mode (see Console Mode Switch section). Further, a WAIT instruction may also be executed by the program without affecting the timers ability to record time correctly.

The timers are started by means of the XIO instruction with the Function of Control referring to Area zero. The IOCC used to start and stop the timer has the following form.

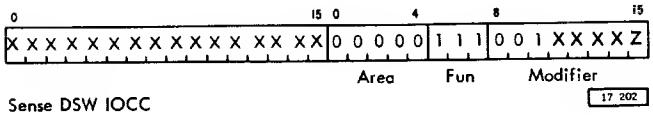


X - Unused

Y - This information is copied into the Timer Control. A one (1) causes the timer to be turned ON and a zero turns the timer OFF. Bit position 0 of the address corresponds to Timer A, Bit position 1 - Timer B, and Bit position 2 - Timer C.

Modifier 001 - Unit Address of Timers

The IOCC used to sense the DSW and reset the interrupt assigned to the timers is shown below.



Sense DSW IOCC

Modifier 001 - Unit Address of Timers

X - Unused

Z - A 1-bit resets the DSW indicators; a 0-bit does not reset them.

The DSW has the following bit significance:

B0	Timer A
B1	Timer B
B2	Timer C
B3-15	Not Used

The bit being ON indicates that the timer has initiated an interrupt.

NOTE: The timers will continue to increment correctly if they are protected with a Storage Protect Bit. However, any other attempt by the P-C or an I/O device to alter the data in a protected timer will cause a Storage Protect Violation.

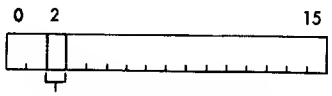
The Storage Protection facility protects the contents of specified locations of core storage from change due to the erroneous storing of information during the execution of a program. This protection is achieved by providing each location in core storage with a Storage Protect bit. The status of each storage location is identified as "read only" or "read/write" by the condition of the Storage Protect bit.

"Read only" is indicated by the bit being set to one (ON). "Read only" is defined as the ability to access a protected location, read the contents into the B-register and regenerate into the storage the contents that were read out. Under program control, any location in core storage may be designated as "read only". Since each location has its own Storage Protect bit, each location is conditioned individually by means of the Store Status instruction.

The Store Status instruction is used to write or clear Storage Protect bits. (See Store Status Instruction description.) The execution of this instruction is under control of the Write Storage Protect Bits switch on the P-C Console. When this switch is ON, the Store Status instruction can change the Storage Protect bits.

Although the Storage Protect bit, the parity bit, and the 16 data bits result in an 18 bit word, only the 16-bit data word need be considered for instruction and data flow purposes. The odd parity bit covers the 16 data bits and the Storage Protect bit. Loss of the Storage Protect bit in a location will be detected by a Parity Check.

Any attempt by the program to write into a "read only" protected location will result in the Internal interrupt (highest priority interrupt). A 2-bit will be placed in the Interrupt Level Status Word (ILSW) of the Internal Interrupt. The data in the protected location will not have been changed.



Storage Protect Position in ILSW for the Internal Interrupt.

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If a Data Channel operation attempts to write into a protected location, the protected data will remain intact and the Storage Protect Violation indicator will be set in a bit position of the Device Status Word (DSW) associated with the device operating on the Data Channel.

This basic feature of the 1800 System can be used to check program operation. If the 1800 P-C fails to execute a predetermined sequence of instructions, an alarm circuit is activated. The alarm may be audible and/or visual (an indicator light is located at the 1800 console). Both the alarming device and the power required to operate it must be furnished by the customer. (Customer power is limited to 30 volts and 3 amperes.)

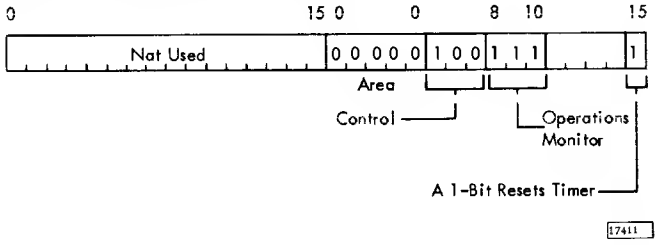
The Operations Monitor includes an interval timer and manual controls on the 1800 console. The operator may select any one of six time intervals: 5, 10, 15, 20, 25 or 30 seconds. (This selection switch is located on the CE panel underneath the console.) Once the Operations Monitor has been activated by the operator, a reset timer command must be executed during program operation at frequent enough intervals to prevent the timer from timing out. If the reset command is not given during the selected time interval, the timer runs out and the alarm circuit is activated. Timeout can also be caused by a power failure, computer hang-up, computer looping, or any departure from the predicted instruction sequence in the program.

Programming Note

The operation of the Operations Monitor depends on the positions of two switches:

1. The Operations Monitor on-off toggle switch on the P-C console.
2. The time interval selector switch on the CE panel.

With these two switches correctly positioned and the P-C in programmed operation, the Operations Monitor timer must be reset at frequent intervals to prevent it from timing out and causing an alarm. An XIO instruction with the IOCC described below is used to reset the timer:



The P-C console (Figure 14) provides the means for manual control of the Processor-Controller during debugging or operating phases.

The basic operating features and controls provide the facility to:

1. Start or stop instruction execution.
2. Address memory.
3. Set-up and store data or instructions.
4. Communicate with the program via Sense or Program Select switches.
5. Control the cycling rate in the Run, Single Memory Cycle, Single Instruction, or Single Stop modes.
6. Interrupt the program manually.
7. Trace each instruction.
8. Reset all control circuitry and storage.
9. Turn power on and off.
10. Indicate basic machine conditions and status.
11. Display memory words and register data.
12. Write or clear storage protect bits.
13. Clear core storage.

Table 5. Clear Storage Functions

Function	Mode Switch	WSPB Switch
1. Store Contents of Data Entry Switches in all Core Storage Locations. Storage-Protect Bits are Removed and Parity is Corrected as Required Because of Bit Removal. If All Data Entry Switches Are Off, Only Parity Bits are Left in Storage.	Run	On
2. Store Contents of Data Entry Switches in Each Core Storage Location that is Unprotected. Locations having Protect Bits are Unchanged.	Run	Off
3. Clear Storage Protect Bits. All Other Data Remains Unchanged. Parity is Automatically Corrected in Each Word in Storage.	Display	On
4. Search for Parity Errors. The P-C Cycles Through Storage Until Stopped by the Stop Key or a Parity Error. The Check Stop Switch Must be on for a Parity Error to Cause a Stop.	Display	Off

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PUSH-BUTTON SWITCHES AND LIGHTS

There are two rows of push-button switches and lights: one row is at the top of the console (Figure 15) and one row at the bottom (Figure 16). Descriptions of their functions follow:

Clear Storage

This push-button (P.B.) switch has four functions (Table 5). None of the four functions can be executed, however, until Clear Storage is first held pressed and then Start is pressed. This dual action requirement prevents the accidental clearing of storage. Note in Table 5 that each Clear Storage function is dependent on the positions of two console switches, the rotary Mode switch and the Write Storage Protect Bit (WSPB) toggle switch.

The P-C cycles completely through all core storage addresses during the execution of each Clear Storage function.

Program Load

This push-button switch is used to load core storage, beginning at location zero, with the first card in the 1442 Card Read Punch or the first tape record in the 1054 Paper Tape Reader. If the 1442 is "ready" when Program Load is pressed, the 80 columns of the first card are stored in the first 80 core storage locations (0000-0079). If the 1054 is "ready" when Program Load is pressed, tape data is read into storage, beginning at location zero, until an end-of-record punch is read.

After reading the first card or tape record, the P-C begins program operation at zero. These first instructions, beginning at zero, must continue the loading operation, including the data for the reserved storage locations (interval timers, index registers, etc.).

The P-C must be in Run mode for program operation to continue after loading.

Ready

This light is on when the P-C is in an operative condition.

Off

This push-button switch is used to shut down the power supplies within the P-C.

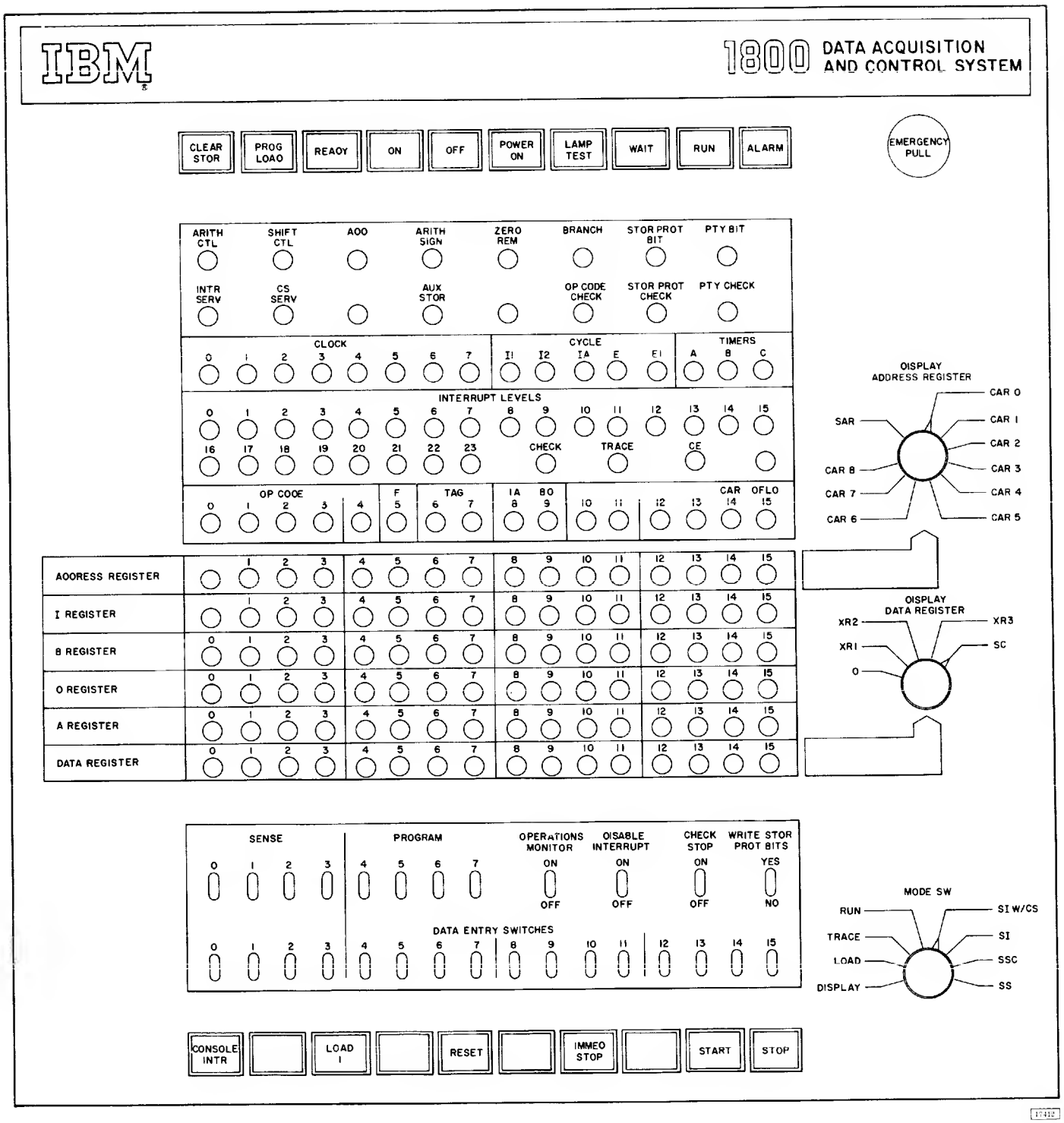

Figure 14. P-C Console

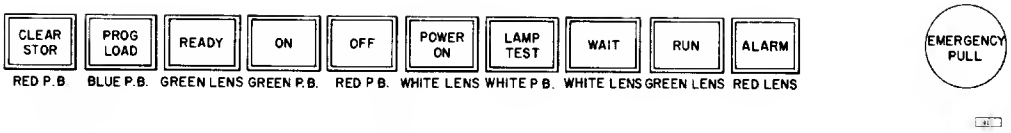

Figure 15. Console Lights and Switches, Top Row

On

This push-button switch is used to turn on the power supplies within the P-C.

Power On

This light is used to indicate that the P-C power supplies are operative.

Wait

This light is used to indicate that the P-C is in either Load or Display mode, or that it has been halted by a Wait instruction.

Run

This light is used to indicate that the P-C is operating under program control.

Alarm

This light is used to indicate that the Operation Monitor has timed out. The customer may install an audible alarm to operate in conjunction with the Alarm light. See Operation Monitor section.

EMERGENCY PULL SWITCH

This pull-switch is for emergency use only. If pulled off, all electrical power within the 1801/1802 is turned off, including power to the blowers that cool the electronic circuitry. Turning the blowers off in this manner may damage some of the circuitry.

Console Interrupt

This push-button switch enables the operator to interrupt P-C operation. The console interrupt level is assigned by the customer. The Program toggle switches may be used in conjunction with Console Interrupt to specify the console interrupt routine. However, this relationship between the Program switches and Console Interrupt would exist only by virtue of the program. There is no internal relationship between the two.

The Console Interrupt IOCC is provided in the Area Code Zero section of the description for the Execute I/O instruction.

Load I

This push-button switch is used with the rotary Mode switch on the Load position to transfer the contents of the Data Entry toggle switches into the I-register of the P-C. The P-C is in the stopped condition when it terminates the Load I operation.

Reset

This push-button switch is used to reset all basic timing, controls, and registers. The Interrupt Mask register is reset with all bits "on."

Immediate Stop

This push-button switch stops the P-C at the end of the 2 or 4 μsec storage cycle in operation when the Immediate Stop contacts close. The Immediate Stop switch can also be used to stop data channel (cycle stealing) operations that are no longer under program control.

Stop

This push-button switch stops the P-C at the end of the instruction in operation when the Stop contacts close. Data channel operations can be stopped only by pressing Immediate Stop.

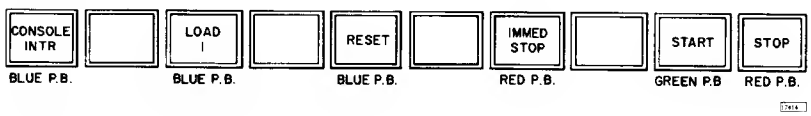

Figure 16. Console Lights and Switches, Bottom Row

Start

This push-button switch initiates P-C operation as specified by the Rotary Mode switch.

Mode Switch

This eight-position rotary switch (Figure 17) is used with the Start switch to extend operator control of the P-C.

Single Instruction with Cycle Steal (SI W/CS). A Start switch depression with the Mode switch on SI W/CS causes the execution of one instruction. Data channel operations can occur during execution of the instruction.

Single Instruction (SI). A Start switch depression with the Mode switch on SI causes the execution of one instruction. Data channel operations are prevented.

Single Storage Cycle (SSC). A Start switch depression with the Mode switch on SSC causes one memory cycle (2 μsec or 4 μsec). Single Storage Cycle operations (usually called Single Cycle operations) can be used in conjunction with the console Cycle lights to step through instructions and analyze P-C operation.

Single Step (SS). A Start switch depression with the Mode switch on SS causes one basic P-C clock cycle (See console Clock Lights).

Run. A Start switch depression with the Mode switch on Run initiates normal program operation of the P-C.

Trace. This position of the Mode switch causes a Trace interrupt prior to the execution of each instruction. The Trace interrupt is a unique interrupt. It has no device status word, no interrupt level status word, and cannot be masked. The Trace interrupt is the lowest priority customer interrupt. Once initiated, it will be delayed by the occurrence of any other interrupt. It can not occur while other interrupts are being serviced. When the Trace interrupt occurs, the P-C executes the forced BSI and branches to the routine whose address is stored at 009. See Interrupt section.

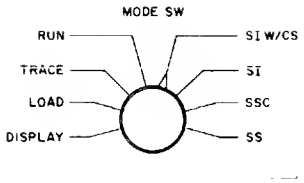

Figure 17. Console Mode Switch

Load. A Start switch depression with the Mode switch on Load causes the contents of the Data Entry Switches to be stored at the address specified by the I-register. (The P-C must be in a stopped condition.) The I-register is incremented following each Load operation caused by pressing Start.

Display. A Start switch depression with the Mode switch on Display causes the data at the I-register address to be displayed in the console B-register lights. The I-register is incremented after each display. Successive words are displayed with successive depressions of Start.

TOGGLE SWITCHES

See Figure 18.

Sense and Program

The contents of these eight switches may be stored in bit positions 0-7 of the A-register or a core storage location. An XIO instruction with an IOCC function of Read stores the contents of the Sense and Program switches at the core storage address specified by the IOCC. (See Area Code Zero in the description of the XIO instruction.) A function of Sense Device stores the switch data in the A-register.

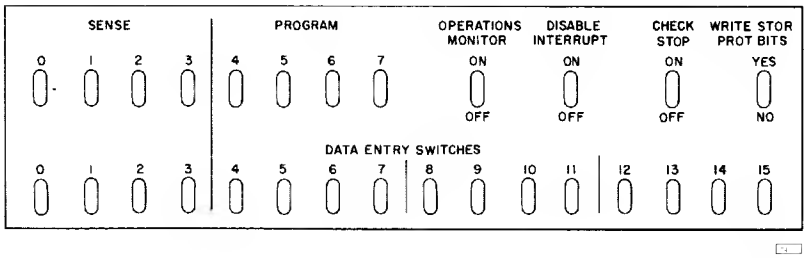

Figure 18. Console Toggle Switches

Operations Monitor

This switch is used to start the Operations Monitor. The off position disables the Monitor.

Disable Interrupt

This switch is used to mask all interrupt levels, including Internal errors. It is especially useful during program analysis when the operator wants to choose the time at which the program may be interrupted. The highest level interrupt on and unmasked is serviced when the switch is turned off.

Check Stop

This switch is used to stop the P-C when an internal error occurs. An internal error is caused by an invalid operation, a parity error, a data channel address register check, or a storage protect violation. The stop occurs at the end of the 2 or 4 μsec cycle that the error is detected. Start must be pressed to restart the system.

An internal error initiates an Internal interrupt when Check Stop is off.

A Clear Storage function is stopped when Check Stop is on and a parity error is detected (see Table 5).

Write Storage Protect Bits

This switch enables the writing or clearing of storage protect bits (see Store Status instruction and Clear Storage functions, Table 5).

Data Entry Switches

The contents of these 16 toggle switches can be stored by either manual or program control. See Area Code Zero in the description of the XIO instruction for program control. The description of the Load position under Mode Switch describes manual control.

CONSOLE INDICATORS

These indicators (Figure 19) show the status of various P-C functions and operations.

Arithmetic Control. On during arithmetic operations.

Shift Control. On during shift operations.

Add. On during add operations.

Arithmetic Sign. On when bit position zero in the A-register (accumulator) does not initially equal bit position zero in the B-register.

Storage Protect Check. Turned on when an attempt is made to write into a "read-only" location.

Parity Check. Turned on when a parity error (even number of bits) is detected in the 18-bit word transfer between the B-register and core storage. The presence or absence of storage protect and parity bits in each word is indicated by their respective console indicators.

Zero Remainder. On when the A-register contains a zero balance during a divide instruction.

Branch. On during branch instructions.

Interrupt Service. Turned on when the hardware BSI instruction is being executed for the highest level interrupt that is on and not masked.

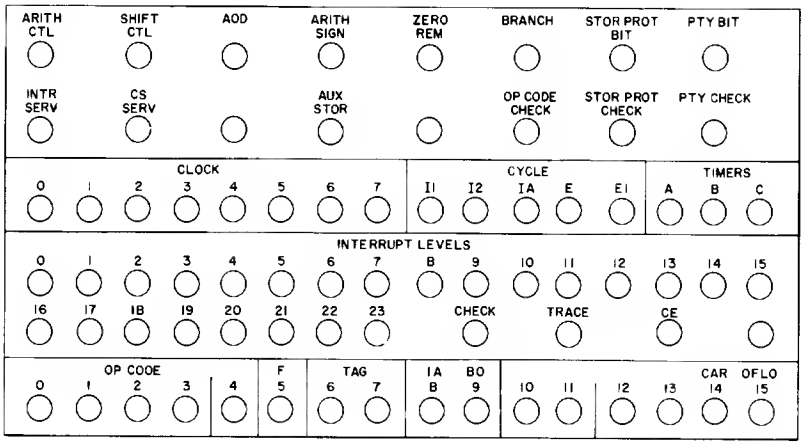

Figure 19. Console Indicators

Cycle Steal Service. On during cycle steal operations for the highest priority data channel requiring service.

Op Code Check. On when an invalid Op code is placed in the Op register.

Auxiliary Storage. Auxiliary storage (256 words for each 4K of Core storage) is provided for Customer Engineering use. The indicator is on when auxiliary storage is being used.

Storage Protect Bit. On when a storage protect bit is transferred with the 16 data bits between the B-register and core storage.

Parity Bit. On when a parity bit is transferred with the 16 data bits between the B-register and core storage.

Parity Checking and Storage Protection

Note that four of the aforementioned console indicators are provided for in these two functions:

1. Storage Protect Check
2. Parity Check
3. Storage Protect Bit
4. Parity Bit

The first two are error conditions which cause an Internal interrupt if the Disable Interrupt toggle switch is off. The last two indicators may be thought of as an extension of the B-register display for parity and protect bits.

Clock

These eight indicators (0-7) show the advance of the basic P-C clock during Start key depressions when the rotary Mode switch is on Single Step (SS). Normally, eight Start key depressions with the Mode switch on SS is equivalent to one Start key depression with the Mode switch on Single Storage Cycle (SSC).

Cycle

These five indicators (I1, I2, IA, E, and E1) show the progress of an instruction that is being Single Stepped or Single Storage Cycled; that is, advanced by successive Start key depressions with the rotary Mode switch on SSC or SS.

I1 shows that a new instruction is being set up for execution. It is turned on at the beginning of all single word instructions and for the first word of all double word instructions.

I2 shows that the second word of a double word instruction is being set up for execution.

IA shows that the instruction being set up is a double word instruction that has an indirect address. The indicator is on while the indirectly addressed word is being read out of storage.

E shows that the instruction set up during I-time has been defined by the Op code and is now being executed.

E1 is turned on with the E indicator. Its on condition shows that instruction exccution control circuitry has progressed to the E1 cycle point. E1 is turned off at the next clock zero (0) time. Instruction can then progress through E2 and E3 time. (There are no E2 and E3 console indicators.)

Timers

These three indicators (A, B, and C) show the status of their respective interval timers. An on condition indicates that the timer is in operation.

Interrupt Levels. An Interrupt Level indicator is on for each interrupt level requesting service or being serviced. Once on, an Interrupt Level indicator can be reset by either of two instructions:

1. A mask instruction that is executed before servicing of the interrupt begins. (The interrupt request is not lost but merely detained until the interrupt level is unmasked, at which time the indicator is turned back on.)
2. A branch-out-of-interrupt instruction is executed to complete servicing of the interrupt.

Both of the abovc instructions are quasi instructions; that is, variations of the XIO and BSC instructions.

The last threc interrupt level indicators — Customer Engineering, Trace and Check (Internal Interrupt) -- cannot be masked. The CE interrupt can be initiated only from the CE panel or from a device operating in CE mode.

Operation Code

These five indicators (0-4) display the Op code of each instruction.

Format (F)

This indicator is on when a two-word instruction is specified.

Tag

The status of these two indicators reflect the instruction register or index register modification of the instruction address, as follows (the on condition of the indicators is shown by a 1):

Indicators 6	7	Register
0	0	I-Reg
0	1	XR-1
1	0	XR-2
1	1	XR-3

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Indirect Addressing

The IA (Bit 8) indicator is on when the instruction contains this bit, which usually indicates indirect addressing.

Branch Out

The BO (Bit 9) indicator is on when there is a bit in position 9 of an instruction. When on in a BSC instruction, a branch-out-of-interrupt is specified.

Carry and Overflow

These two indicators are turned on individually when their respective conditions occur in the accumulator (A-register).

DATA FLOW DISPLAYS

Six rows of indicators and two rotary switches (Figure 20) facilitate the display of data flow in the P-C. A review of the P-C Data Flow section and the Data Channel section is recommended at this point.

Address Register

These 16 indicators display the data in the Storage Address Register (SAR) or the selected Channel Address Register (CAR), depending on the position of the Display Address Register rotary switch. The selected register is displayed each time the P-C comes to a stop or wait condition.

Display Address Register Switch

This 10-position rotary switch is used to select a CAR or SAR for display in the Address Register.

Permanent Register Displays: I, B, D, and A

The contents of these four registers are always displayed.

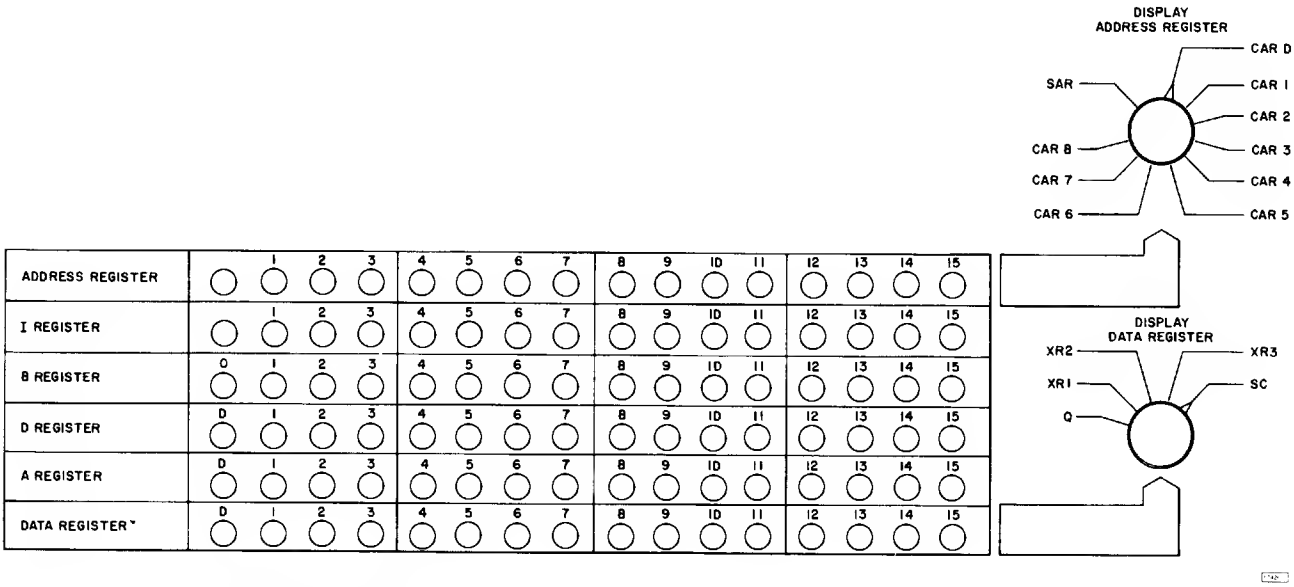

Figure 20. Data Display Lights and Switches

Data Register

These 16 indicators display the contents of the Q-register, which is the accumulator or A-register extension, the index registers (XR1, XR2, or XR3), or the shift counter (SC), depending on the position of the Display Data Register rotary switch. The selected register is displayed each time the P-C comes to a stop or wait condition.

Display Data Register Switch

This 5-position rotary switch is used to select the Q-register, an index register, or the shift counter for display in the Data Register.

DISPLAY PROCEDURES

The following procedure may be used to display core storage data between the execution of single instructions:

1. With the P-C in a stop condition, position the rotary Mode switch to SI (Single Instruction).
2. Start switch depressions may now be used for single instruction operations to get the program to the desired point for data display.
3. Record the address in the I-register. (The I-register is used in Display mode and this recorded address will be needed to return the P-C to the next instruction.)
4. Set the address of the core storage word to be displayed in the Data Entry Switches.
5. Position the Mode switch to Load.
6. Press Load I switch.
7. Position Mode switch to Display.
8. Press Start. The selected word is now displayed in the B-register indicators.
9. To display other core storage words, repeat steps 4 through 9.
10. To continue the program:
    a. Set Data Entry Switches to address recorded in step 3.
    b. Position Mode switch to LOAD.
    c. Press Load I switch.
    d. Position Mode switch to RUN.
    e. Press START.

To display core storage data between single memory core operations:

1. With the P-C in a stop condition, position the Mode switch to SSC (Single Storage Cycle).
2. Press Start repeatedly until the desired cycle in the execution of the instruction is reached.
3. Perform steps 3 through 10 of the preceding Single Instruction execution procedure.

There are two basic methods of transmitting and/or receiving data to or from the P-C. First, specific low speed devices are controlled directly by the program. In this Direct Program Control operation each character or word of data is transmitted to or from the P-C core storage by means of separate Execute I/O (XIO) instructions. The program continues transmission, character by character, or word by word, by responding to "Service Request" interrupts. Devices operating under Direct Program Control (DPC) include:

1816 Printer Keyboard
1053 Printer
1627 Plotter
1054 Paper Tape Reader
1055 Paper Tape Punch
Process I/O Devices such as analog-to-digital converters, contact sense, voltage level sense, pulse counters, etc.

The second method of transferring data is via the Data Channels. Data channel (DC) operations are initialized by a single XIO instruction. The transfer of data words then proceeds under control of the specified DC, completely asynchronous to program operation.

The Data Channel's method of accessing core storage provides a powerful means of I/O communication with the core storage. Whenever the DC requires core storage access, the P-C operation is suspended for one core storage cycle time. During this cycle the data is taken from or placed into core storage. Access by the DC can occur at the end of any memory cycle. It does not require that an instruction be completed. As soon as the DC has been satisfied, which normally takes one cycle, the stored program execution proceeds. The logical state of the P-C is not changed by the DC's access to core storage. This method of access is sometimes referred to as "cycle stealing" since a cycle is taken from the stored program execution cycles at any time.

Devices operating under DC control include:

2401/2402 Magnetic Tape Drive
2310 Disk Storage Drive
1443 Printer
1442 Card Read-Punch
System/360 Adapter

Some devices operate under DC or DPC control, depending on their characteristics and the configuration of the 1800 system. These devices include:

Analog Input
Analog Output
Digital Input
Digital Output

Detailed descriptions of DPC and DC operations follow.

DIRECT PROGRAM CONTROL OPERATION

DPC operation of I/O devices proceeds on a one for one basis; that is, an XIO instruction is executed for each data word transferred to or from core storage. The XIO instruction for DPC specifies an I/O Control Command (IOCC) with a function of Control, Sense Interrupt Level, Sense Device, Read or Write. (See description of XIO instructions.)

Control. An IOCC with a function of Control uses the IOCC address and modifier to specify the particular device and the operation to be executed. Examples of Control operations are Load Multiplex Address, Feed Card, and Load Interrupt Mask Register.

Sense. An IOCC with a function of Sense Interrupt Level or Sense Device is used to read the "status words" associated with the device: the Device Status Word (DSW), the Process Interrupt Status Word (PISW), and the Interrupt Level Status Word (ILSW). These status words are explained in detail in the Interrupt section. Generally, DSW's are associated with data processing I/O units (card reader, card punch, etc.) and PISW's are associated with industrial processing interrupts (excessive temperature, overflowing tank, etc.). An ILSW is provided for each interrupt level.

Read or Write. An IOCC with a function of Read or Write uses the IOCC address to determine the core storage address receiving or providing the single data word. Immediately following the one word transfer to or from storage, the XIO instruction is terminated and the next sequential instruction is executed. Normally, several data words must be transferred to

complete the message transfer. This is accomplished by P-C recognition of a device interrupt each time the device is ready to send or receive a data word. P-C recognition of the interrupt causes a branch to a program subroutine associated with the device interrupt. The interrupt subroutine includes the XIO instruction to read or write the next data word. This subroutine must also modify the address portion of the IOCC for the next data word, provide "table look up" for translation of the device character if required, and maintain a program word count to indicate the end of message if necessary.

The exit from the interrupt subroutine must be accomplished with a BSC instruction that has a bit in its BO or Bit 9 position. This Branch-Out-of-Interrupt operation restores the interrupt hardware so that future interrupt requests at the same or lower priority levels can be acknowledged.

Device Busy

It is possible for the program sequence to execute an XIO instruction to a device that is busy responding to a previous XIO instruction. Each device that can have this condition will provide a Busy indicator in the DSW. This indicator signals that the device cannot accept data or control information, and that should it be sent it will be lost. It is up to the program to insure, by testing the Busy indicator, that data will not be lost. Except for the System/360 Adapter, no hardware indication is given to signal incorrect use of the device.

Data Overrun

It is possible for a device operating asynchronously to the program to request a data word transfer before the program sequence is ready to service the request. This can be true for both input and output. Devices with this potential must provide a "program check" indicator that will enable the P-C to know if a data overrun occurs.

DATA CHANNEL OPERATION

Data channels are used to transfer data between P-C core storage and high speed I/O devices. The P-C initializes each DC with a single XIO instruction. The DC then takes control of the data transfer while the P-C continues program operation. The DC has priority to the extent that when the I/O device is ready to send or receive a data word, the P-C is stopped while the word transfers to or from core storage. This transfer takes 2 or 4 μsec, depending on the core storage cycle time, and is referred to as a cycle steal. P-C data and conditions are undisturbed except for the core storage locations that receive data from an input device.

Three DC's are standard on the 1800 system; six more are available on an individual basis. Thus, it is possible to have more than one I/O device requesting core storage cycles at the same time. When this occurs, the DC control circuitry stops the P-C and services the requesting devices according to their DC priority. This priority is a hardware priority assigned by the user and is not related in any way to the Interrupt feature. The maximum time before service of the highest priority DC (level zero) is 2.25 or 4.5 μsec, depending on the cycle time of core storage. After all requesting devices have been serviced, the P-C continues with the program.

I/O devices that are to be operated concurrently must be on separate DC's. Those that do not require concurrent operation can be on the same DC.

Functional Components

Data Channels include the following components:

Channel Address Register (CAR) - one per DC
Channel Address Buffer (CAB) - one for all DC's
Control Circuitry

I/O devices have the following registers for DC operation:

Word Count Register (WCR)
Scan Control Register (SCR)

Data Channel Control

Data Channel initialization begins with the execution of an XIO instruction. The numbered steps that follow correlate with the circled numbers in Figure 21:

1. The XIO references the IOCC.
2. The Area and Modifier of the IOCC specify the I/O device. The DC and its CAR are selected at the same time by virtue of their connection to the I/O device. The Function (Initialize Read or Initialize Write, etc.) specifies the operation.
3. The Address portion of the IOCC is stored in the CAR for the selected DC. Each DC has its own CAR. The XIO instruction is terminated and the P-C continues program operation at this point.
4. As soon as the device requests a data transfer, the first cycle steal begins. The P-C is stopped at this point. The address in CAR is transferred to the Channel Address Buffer (CAB). There is one CAB for all CAR's.

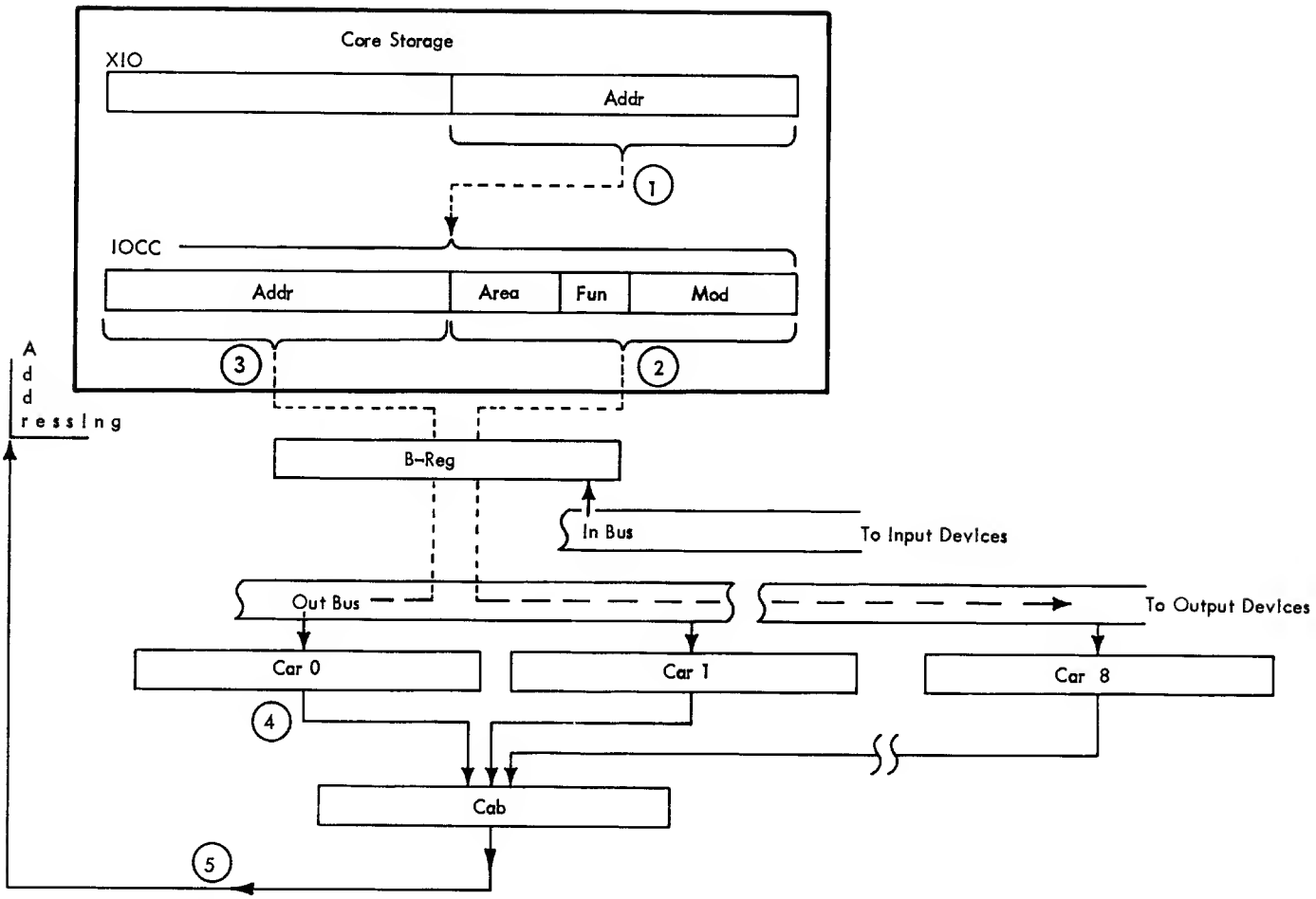

Figure 21. Initialization of Data Channel Operation

5. CAB addresses core storage for the first word of the data table while CAR is being incremented. (Steps 6 through 8 are shown in Figure 22.)
6. The first word of the table, which was addressed in step 5, contains the scan control bits (bit positions 0 and 1) and the word count (bit positions 2-15).
   a. The scan control bits are sent to the Scan Control Register (SCR) in the I/O device. The SCR indicates what the I/O device and the DC should do when the end of the data table is reached, as follows:

Bit Positions		
0	1	Single scan of Data Table and stop with an interrupt.
0	1	Single scan of Data Table and stop (no interrupt).
1	0	Continuous scan of this table or difference tables with an interrupt at the end of this table.
1	1	Continuous scan of this table or different tables with no interrupt.

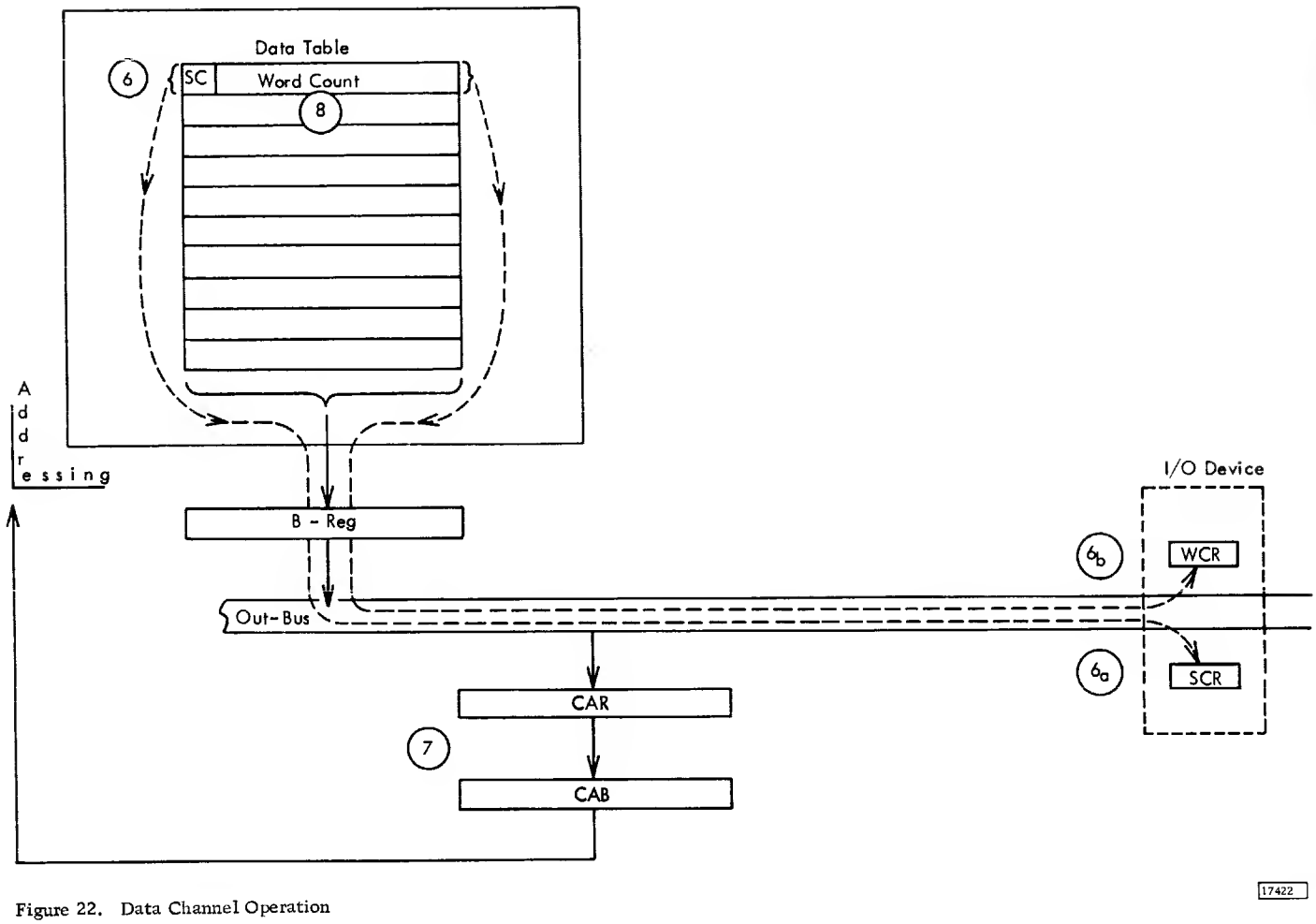

Figure 22. Data Channel Operation

(The ability to chain in a continuous scan of the same or several different tables is a function of the I/O device. A device need not have chaining ability in order to interrupt at the end of the data table.)

b. The Word Count is sent to the Word Count Register (WCR) in the I/O device. This ends the first cycle steal.

7. When the device requests a storage access, CAR, which was incremented in step 5, now transfers the next higher address to CAB. CAB addresses core storage while CAR is being incremented.
8. The first data word is transferred to or from the I/O device via the B-register and the DC. The WCR in the I/O device is decremented by one. This is the end of the second cycle steal.

Steps 7 and 8 now continue on a cycle steal basis; that is, they occur as the I/O device requests data transfers. Between cycle steals, the P-C continues program operation. The CAR is incremented with each data transfer and the WCR is decremented. This sequence continues until the last data word of the data table is transferred. The last word transfer is sensed by the WCR reaching zero or through some indicator in the device. If the device does not have chaining ability, no more demands for data transfer are made until the device is reinitialized with another XIO instruction.

Data Chaining

When a continuous scan is indicated by the Scan Control Register (SCR) in a device having chaining ability, the DC takes two cycles after the WCR has reached zero. The first cycle is used to transfer the word following the data table to the CAR. The address in this word is the address of the next table of data. The first word of the new table contains the scan control bits and the word count, both of which are immediately transferred by the device to the SCR and the WCR. The device then requests the second word of the new table and the independent operation of the DC

proceeds as before. In this manner, the DC can operate in a scatter read-write mode. This method of using the DC in a continuous mode is called "data chaining" because the data tables are essentially connected together. The length of time between data transfer cycles on a data chaining operation is a maximum of four memory cycles on a device connected to the highest priority DC. It may be greater than this for devices of lower cycle steal priorities, depending on whether they must wait for higher DC priorities to be serviced.

Data Table

An example of a data table is shown in Figure 23. (The location of the XIO instruction is immaterial in this example.) Note that the IOCC is located at the end of the data table. Although this need not be — the IOCC can be located anywhere in corc storage — there is a savings of one core storage position in this example. The savings occurs because the scan control bits specify a continuous scan and the desired scan is a repeated scan of the same table. A continuous scan operation requires that the word immediately following the data table contain the address of the next table. Therefore when the same table is to be scanned again, it is expedient to have the IOCC address located for this purpose. The address portion of the IOCC is then used not only to address the data table the first time, but to address it for the continuous scan as many times as required.

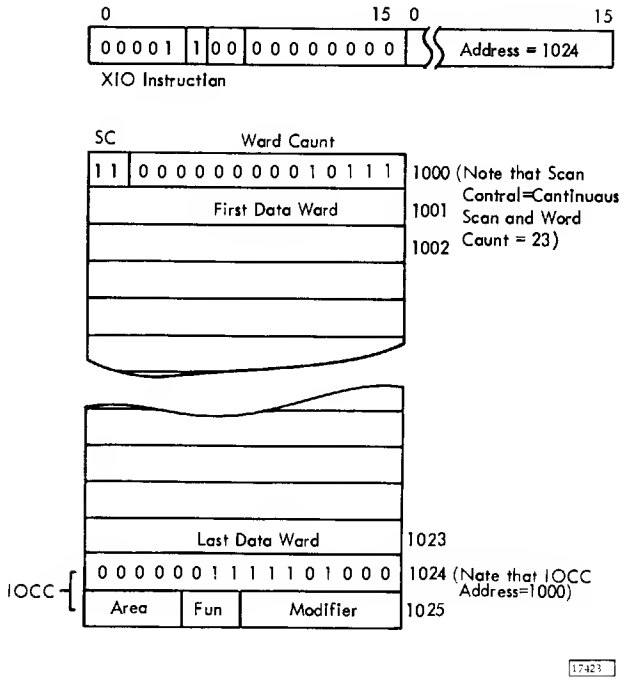

Figure 23. Data Table

The Interrupt feature provides an automatic branch from the normal program sequence based upon an external condition. Examples of conditions which would normally be used to cause interrupts follow: (1) The Interval Timer has concluded the recording of a preset time interval. (2) The Magnetic Tape drive initialized and selected on a Data Channel has completed the required data transfer and signals the P-C with a Scan Complete. (3) An undefined operation code has been detected during the P-C instruction readout and therefore cannot be executed. (4) A device, such as the typewriter, has completed the transfer of the previous character and requests a subsequent character. (5) An external process condition has been detected which requires an immediate change in the program execution.

Interrupt Philosophy

Because of the large number and widely varying types of interrupt requests, it is often not desirable to cause a branch to a unique address for each condition. For the same reasons, it is frequently not desirable to cause one branch for all interrupt requests and require the program to determine the individual request(s) requiring service. Therefore, it is expedient to group the many individual request lines into a lesser number of priority levels. This accomplishes two very important functions: First, it allows all interrupt requests common to a specific interrupt level to have the privilege of interrupting immediately if the only requests present are of a lower priority level. Conversely, it permits interrupt requests connected to a higher priority level to temporarily terminate the servicing on a lower level and immediately interrupt to the higher priority. Service is returned to the initial request only after all higher level requests have been serviced. Second, since a unique branch can be defined for each interrupt priority level, it is possible to combine many interrupt requests on a common priority level and therefore use a common interrupt subroutine to service many requests.

There are two important operating characteristics of the interrupt system. (1) When more than one request line is connected to any priority level, it is necessary by programming means to identify the individual request(s) causing the priority level to be energized. (2) The first request that is recognized on a given priority level prevents future requests on that or lower priority levels from interrupting until the completion of servicing the first interrupt is signaled by a Branch Out Operation (see Branch or Skip on Condition-BSC). However, interrupts that occur on the same level for which an interrupt is being serviced can be interrogated and serviced by programming if the Interrupt Level Status Word (ILSW) is interrogated again before the "Branch Out" is executed. The ILSW is explained in detail towards the end of this section.

INTERRUPT LEVELS

As shown in Table 6 a maximum of 24 external interrupt levels are available. Twelve external interrupt levels are standard, as are the Internal, Trace, and CE interrupt levels. Note that the priority level of each interrupt is listed as well as its unique core storage address in decimal form. Note also that all but the Trace and CE interrupts have an Interrupt Level Status Word (ILSW). The ILSW, which is explained in detail later, is used to identify the

Table 6. Interrupts

Interrupt	Priority Level	Decimal Address	ILSW	
Internal	0	8	Yes	
Trace	25	9	No	
CE	26	10	No	
External 0	1	11	Yes	
1	2	12	Yes	
2	3	13	Yes	
3	4	14	Yes	
4	5	15	Yes	Basic
5	6	16	Yes	
6	7	17	Yes	
7	8	18	Yes	
8	9	19	Yes	
9	10	20	Yes	
10	11	21	Yes	
11	12	22	Yes	
12	13	23	Yes	
13	14	24	Yes	
14	15	25	Yes	Special Feature Group 1
15	16	26	Yes	
16	17	27	Yes	
17	18	28	Yes	
18	19	29	Yes	
19	20	30	Yes	Special Feature Group 2
20	21	31	Yes	
21	22	32	Yes	
22	23	33	Yes	
23	24	34	Yes	

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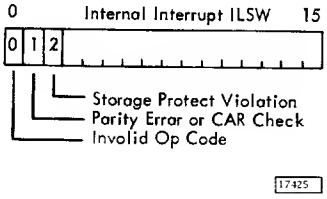
specific condition causing its interrupt level to request service.

Internal Interrupt

The Internal Interrupt is a P-C interrupt that occurs when any one of three error conditions occur in the P-C:

1. An invalid Op code is detected.
2. A parity error (even number of bits) is detected in the B-register during data transfer to or from from core storage, or a CAR check occurs.
3. A storage protect violation occurs from an attempt to write into a "read-only" core storage position.

The Internal interrupt cannot be masked. Its ILSW is reset when it is sensed to determine the interrupting condition. The three error conditions are assigned to the ILSW as follows:



Trace Interrupt

The Trace interrupt occurs after every instruction if the P-C is in program operation with the console Mode switch on Trace. The Trace interrupt cannot be masked and does not have an ILSW.

CE Interrupt

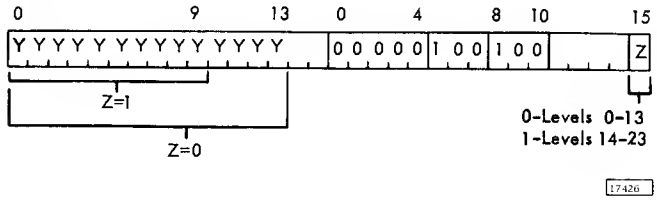
The CE interrupt can be initiated from the CE panel or from a device operating in CE mode. It cannot be masked and does not have an ILSW.

Interrupt Level Masking

A mask register exists for the masking and unmasking of external interrupt levels. An interrupt level that is masked cannot initiate a request for service until it has been unmasked. Any interrupt condition occurring while its level is masked will be retained until the level is unmasked, at which time the request will be recognized in a normal manner.

The XIO Control instruction is used to simultaneously mask and unmask external interrupt levels 0-13 or 14-23, depending on Modifier bit 15 of the IOCC. Two XIO Control instructions are required to mask/unmask the maximum of 24 external interrupts. (All external interrupts are automatically masked when electrical power is first applied to the P-C.) The execution of this instruction does not affect the contents of the A-register.

The IOCC for the Mask instruction is shown below:



Note that the Area is 00000 and that Modifier bits 8-10 must be 100.

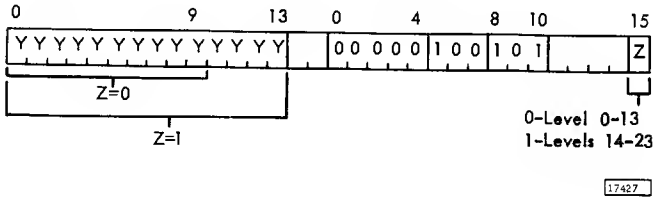
The status of Address bit positions 0-13 or 0-9, depending on Modifier bit 15 (Z), determine whether external interrupt levels 0-13 or 14-23 are masked or unmasked:

A 1-bit masks the corresponding interrupt level.

A 0-bit unmasks the corresponding interrupt level.

Programmed Interrupts

External interrupt levels can be programmed. An XIO Control instruction is used to turn on individual external interrupt levels within either of two groups, 0-13 or 14-23, depending on the status of Modifier bit position 15 of the IOCC. Two instructions must be executed to turn on interrupt levels in both of these groups. The IOCC is shown below:



Note that the Area is 00000 and that Modifier bits 8-10 must be 101.

The status of Address bits 0-9 or 0-14, depending on Modifier bit 15 (Z), determine whether individual interrupts within priority levels 0-13 and 14-23 will be turned on:

A 1-bit turns on the corresponding external interrupt level.

A 0-bit does not turn on the corresponding external interrupt level.

STATUS WORDS

The I/O devices of the 1800 system and some of the system features contain "status" indicators. The on/off condition of each status indicator reveals to the operating program an operational status or condition of the device in which the indicator is located. Status indicators are also contained in the process being monitored and/or controlled by the 1800 system. These indicators, both system and process oriented, project their individual conditions into the system via the In-Bus. Those process and system indicators assigned to interrupt levels initiate interrupt requests when they are turned on.

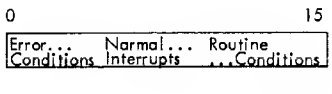
An XIO Sense Device instruction, which specifies a particular device, is used to read into the A-register the on/off condition of each indicator located in the specified device. Once the indicators of the specified device are read into the A-register, the contents of the A-register are considered a Device Status Word (DSW) or a Process Interrupt Status Word (PISW), depending on whether the device is located within the system or in the process. The content of the A-register is considered a DSW when the bits represent the status of indicators from a system device. The content of the A-register is considered a PISW when the bits represent the status of the process interrupts.

DSW Indicators

DSW indicators usually fall into three general categories:

1. Error or exception interrupt conditions.
2. Normal data or service required interrupts.
3. Routine status conditions.

The assignment of indicators to DSW bit positions is usually specified from left to right in the following manner:



All DSW's are shown in Table 7.

When the DSW indicators are read into the A-register by an XIO Sense Device instruction, bit position 15 of the IOCC referenced by the XIO Sense Device instruction determines whether the indicators are reset when their status is read into the A-register. If a bit is present in position 15 of the IOCC, the indicators are reset.

PISW Indicators

The PISW indicators, which are physically located in the 1800 System, are turned on by contact closures or voltage shifts in the process. The principal differences between PISW indicators and DSW indicators are:

1. When an XIO Sense Device instruction reads the specified PISW, the indicators are unconditionally reset. (Bit 15 of the IOCC is used to determine reset of the DSW indicators.)
2. There are restrictions on the assignment of process contacts to PISW's and PISW bit positions. This is because of the manner in which process interrupts are terminated in the 1800 system.

Assignment of PISW Bit Positions

Process interrupts are terminated on 16-position terminal blocks within the 1800 system. The terminating circuitry restricts the assignment of process interrupts to both individual PISW's and the bit positions within each PISW:

1. Terminal block positions 0 through 15 must be assigned to corresponding PISW bit positions 0 through 15. There can be no cross assignment, such as position 0 of the terminal block to position 1 of the PISW. Position 0 must be assigned to position 0, 1 to 1, ... 15 to 15.
2. Terminal block positions can be separated in groups of four and assigned to one, two, three, or four PISW's.

For example, as shown in Figure 24, terminal block positions 0-3 may be assigned to bit positions 0-3 of one PISW; terminal block positions 4-7 may be assigned to positions 4-7 of a second PISW; terminal block positions 8-11 to 8-11 of a third PISW; and terminal block positions 12-15 to 12-15 of a fourth PISW. In like manner, terminal block positions 0-7 could be assigned to 0-7 of one PISW, and terminal block positions 8-15 to 8-15 of a second PISW.

Twenty-four PISW's exist in the 1800. They are addressed individually by the modifier of the XIO Sense Device instruction. PISW decimal addresses in the modifier are 2 through 25.

Interrupt Level Status Word

The Interrupt facility includes one 16-position Interrupt Level Status Word (ILSW) for each interrupt level. (The Trace and CE interrupts are exceptions; they are unique interrupts and require no ILSW.) Like the PISW and the DSW, the ILSW is not actually a word

Table 7. Device Status Words

AREA	FEATURE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Console Interrupt	* Interrupt Request															
	Interval Timers A-125μs, B-1ms, C-64ms	* Timer A	* Timer B	* Timer C													
1	1816 Printer - Keyboard	* Typewriter Service Request	* Keyboard Service Request	* Keyboard Request		Typewriter Busy	Typewriter Not Ready	Keyboard Not Ready	Storage Protect Violation	Keyboard Parity Error	Printer Parity Error			CE Busy	CE Not Ready		
	1053 Printer	* Service Request				Busy	Not Ready				Printer Parity Error			CE Busy	CE Not Ready		
2	1442 Card Read Punch			Error	Last Card	* Operation Complete	Parity Error	Storage Protect Violation						CE Busy	CE Not Ready	Busy	Not Ready
3	1054/1055 Paper Tape Reader/Punch	Reader Any Error	* Reader Service Request	Punch Parity Error	* Punch Service Request	Reader Busy	Reader Not Ready	Punch Busy	Punch Not Ready	Reader Parity Error	Reader Storage Protect	CE Reader Busy	CE Reader Not Rdy	CE Punch Busy	CE Punch Not Rdy		
4	2310 Disk Storage	Any Error	* Operation Complete	Disk Not Ready	Disk Busy	Home	Parity Error	Storage Protect Violation	Data Error	Write Select	Data Overrun		CE Not Ready	CE Busy		Sector Count High	Sector Count Low
5	1627 Plotter	* Service Request	Parity Error											CE Busy	CE Not Ready	Busy	Not Ready
6	1443 Printer	* Transfer Complete	Error	* Printer Complete	Channel 9	Channel 12	Channel 1	Parity				CE Carriage Busy	CE Printer Busy	CE Not Ready	Carriage Busy	Printer Busy	Not Ready
10	Analog Input Basic	* End of Table	* DPC SS Conv Complete	* DPC Rly Conv Complete	* Storage Protect Violation	* Parity Control Error	* Parity Data Error	* ADC Overload	* Overlap Conflict	Cyc Steal, SS, ADC Busy	DPC Busy						Any Error
	Comparator	* High Out of Limit	* Low Out of Limit	* Overload	SS MPX			AMAR 512	AMAR 256	AMAR 128	AMAR 64	AMAR 32	AMAR 16	AMAR 8	AMAR 4	AMAR 2	AMAR 1
11	Digital Input Basic	* Parity Error	* Storage Protect Violation	* DI Scan Complete													DI Busy
	PISW	← Process Interrupt Points →															
12	Digital and Anolog Output Basic	* Parity Error	Pulse Output Timer	* D & A Out Scan Complete													D/AO Busy
14	2402 Mag Tape		Tape Unit Select	Command Reject	* End of Table	Chain Stop	Storage Protect Violotion Stop	Tape Data Error	Parity Error	Data Overrun	* Operation Complete	Tape Diagnostic Error	Wrong Length Record	At Load Point	Tape Indicator or Mark	Tape Channel Busy or Rewind	Tape Channel Busy or Not Ready
13	S/360 Adapter	* Command Reject	1800 Command Stored	360 * Command Stored	* Halt	* Data Check	* Storage Protect	* Transfer End		← 360 Command →							
	Adapter Word Counter	← Word Counter →															

*Interrupt Conditions

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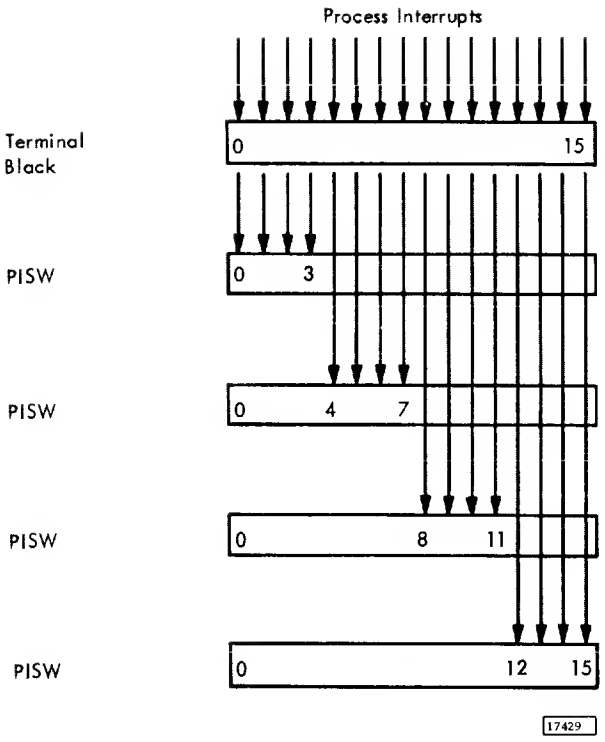


Figure 24. Bit Positions Assignment of PISW's

until it is read into the A-register. Prior to its entry into the A-register, an ILSW is simply 16 signal lines, each of which has OR'ed to it indicators from a status word (PISW or DSW). This relationship is shown in Figure 25.

Each interrupt level requests service when any one of the 16 bits in its ILSW is turned on. When the P-C program recognizes the interrupt request, it executes an XIO Sense Interrupt Level instruction to read the ILSW of the requesting interrupt level into the A-register. The P-C program then determines which bit position in the ILSW caused the interrupt. This bit position identifies the DSW or PISW that has the interrupt initiating indicator. The DSW or PISW is then analyzed by the P-C program to determine which indicator in the DSW or PISW caused the interrupt.

The programmer does not specify the ILSW in the XIO Sense Interrupt Level instruction used to read the ILSW into the A-register. This specification is fixed; that is, each ILSW is hardware assigned to its interrupt level. The Sense Interrupt operation provides the ILSW of the highest priority level requesting service. Except for the P-C Internal interrupts, none of the DSW and/or PISW interrupt indicators ORed into ILSW bit positions are reset when the ILSW is read into the A-register. The indicators are not reset until their respective DSW or PISW is read into the A-register with an XIO Sense Device instruction.

Figure 25 also shows that each PISW may be assigned to one bit position of an ILSW. If this practice were carried to its extreme, all 24 PISW's could be assigned to only two ILSW's, which would restrict all process interrupts to two interrupt levels. Conversely, only one PISW could be assigned to each ILSW, which would provide the maximum number of interrupt levels for process interrupts.

PROGRAMMED OPERATION

The 1800 system may be programmed to service interrupt requests in several alternative manners:

1. Process and other interrupts are intermixed on the same level. The ILSW is interrogated first and the PISW is interrogated subsequently.
2. Process and other interrupts are intermixed on the same level, but process interrupt is given

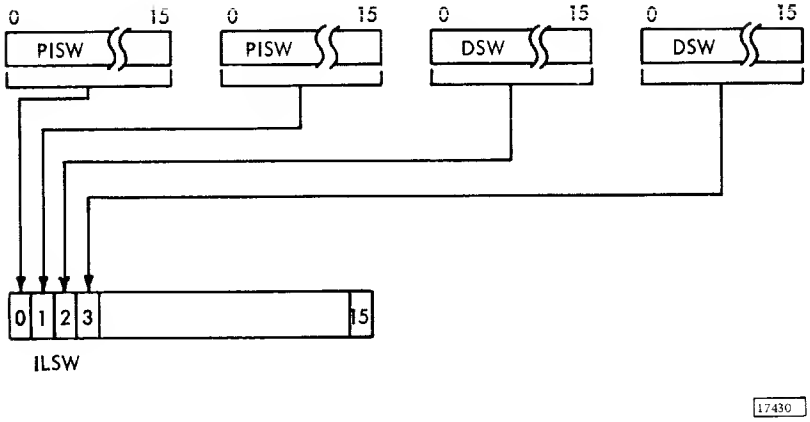


Figure 25. Relationship of Status Words

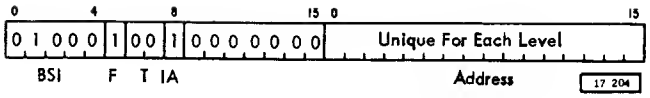
priority on that level so that the PISW's (typically one) are sensed directly and checked before the ILSW is sensed and checked.

3. An interrupt level is completely reserved for process interrupts and interrogation of the ILSW determines which PISW contains the actual interrupt.
4. An interrupt level is completely reserved for process interrupts and the number of PISW's on that level is restricted to one. In this case, the program can go directly to the PISW containing the interrupting condition.

In general, an interrupt request is recognized at the completion of the instruction being executed when the interrupt request occurs. Exceptions to this practically instantaneous recognition occur when:

1. The instruction being executed when the interrupt request occurs is either an interrupt forced Branch and Store Instruction Register (BSI) instruction or a Programmed Interrupt instruction that affects the interrupt request.
2. The interrupt request level is masked. The request will be retained for recognition when the interrupt level is unmasked.
3. The interrupt request is of the same or a lower priority level than an interrupt level being serviced.

When an interrupt request is recognized, the P-C inhibits the normal access to core storage and generates into the B-register a BSI Indirect Addressing instruction. The format of this forced hardware instruction is:



Programming Details

The Address of the forced BSI Indirect instruction is unique for each interrupt level, as specified in Table 6. Program operation from this point is shown in Figure 26 and described below. (The circled numbers in Figure 26 correspond to the numbered descriptions below:

1. The interrupt request occurs during operation of the main line program.
2. The forced BSI Indirect instruction stores the contents of the I-register at the Effective Address (EA) of the instruction. The EA is the address that the user stores at the interrupt level's unique address (Table 6). The forced BSI Indirect instruction then branches to the address of the interrupt subroutine (EA + 1).
3. The interrupt subroutine stores all data and/or index registers that it will use and then prior to subroutine completion restores the same data and/or index registers.
4. The last instruction of the interrupt subroutine is a Branch or Skip on Condition (BSC) instruction (with a BO bit) that returns the program to the address previously stored at the EA (step 2). This address is the location of the next instruction in the main line program. The BSC (with BO bit) instruction also resets the interrupt level so that other lower priority levels can be recognized.

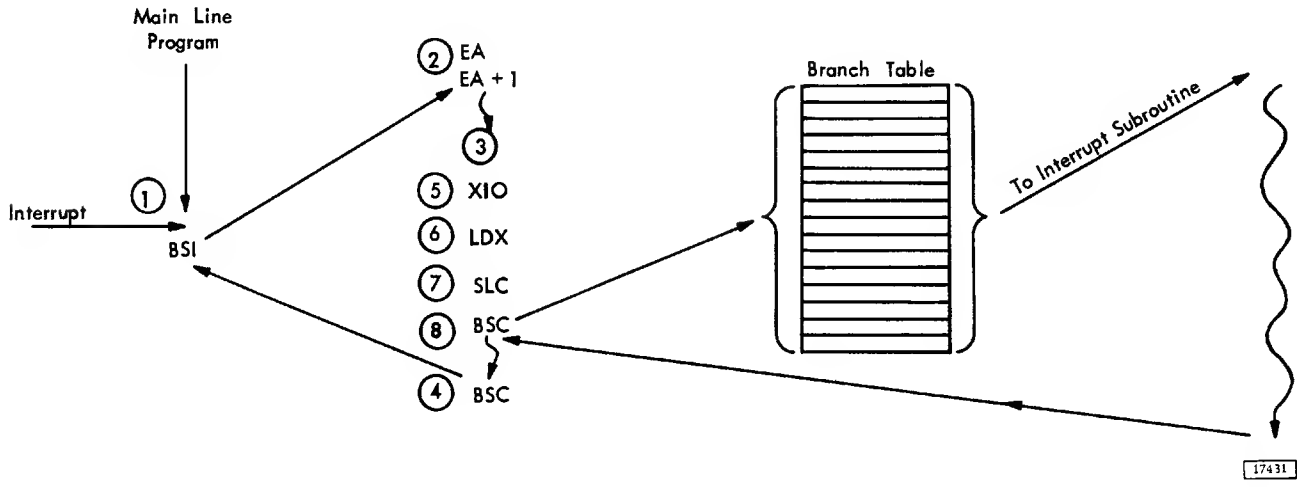


Figure 26. Program Identification of Interrupts

If a Wait instruction is operative when the interrupt request occurs, the Wait instruction is considered complete when the interrupt request is recognized. Following completion of the interrupt subroutine, the instruction immediately following the Wait instruction will be executed.

Because a number of interrupt requests can be assigned to any one priority level, program analysis of the requesting interrupt level's ILSW is necessary to determine the source of the interrupt request signal. This analysis is accomplished within the interrupt subroutine in the following manner (the numbered descriptions that follow relate to the circled numbers in Figure 26):

5. An XIO Sense Interrupt Level instruction causes the ILSW for the interrupt level being serviced (the highest priority level on) to be read into the A-register. Only the Function of the IOCC need be specified. No other parts of the IOCC are used. The status of the indicators in the devices assigned to the ILSW are not reset.
6. A Load Index Register (LDX) instruction loads an index register with the number of interrupt signals assigned to the ILSW.
7. A Shift Left and Count (SLC) instruction is executed. The resulting count in the index register corresponds to the first non-zero bit of the ILSW in the A-register.
8. A BSC instruction is executed. This instruction is both indirect and indexed with the index register containing the count corresponding to the first non-zero bit in the A-register. The Address of the BSC instruction is related to the bottom word of the Branch Table (Figure 27).

   The Branch Table is a table of addresses. Each address is the location of an interrupt subroutine that is related to an interrupt request assignment in the ILSW. Thus, if bit position zero of the ILSW is on, the last word of the table is used, and the BSC branch is to the address stored in the last word of the table.

   If bit position one of the ILSW is on, the BSC branch is to the address stored in the second to last word of the Branch Table, etc.

Thus the above sequence of instructions locates the interrupt subroutine for the ILSW bit that initiated the interrupt. Each time the A-register is shifted, the shift count is decreased by one. As the shift count is decreased, the indexed address for the BSC instruction is decreased. Effectively, the branch

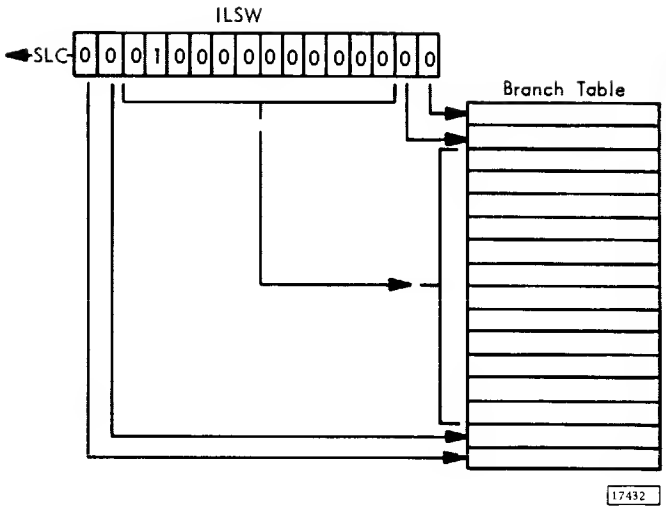
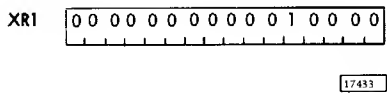


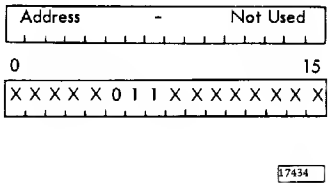
Figure 27. ILSW Branch Table

address of the BSC instruction begins at the bottom of the Branch Table and progresses up the Branch Table as the A-register is shifted. For example:

1. Load Index Register
   Index Register one (XR1) is loaded with sixteen or the maximum number of interrupt request lines connected to the level which caused the interrupt. (In this example, assume sixteen request lines are connected to the interrupting level.)

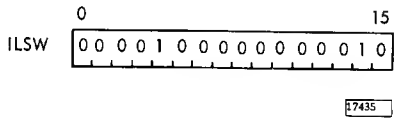


2. Execute I/O (Sense Interrupt Level)
   An XIO instruction is executed which senses the ILSW of the interrupting level into the A-register.
3. I/O Control Command



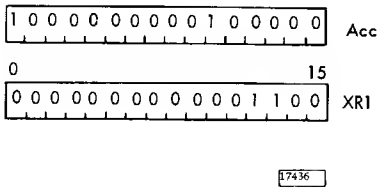
X - Unused bits

In this example, the ILSW appears in the A-register as follows:



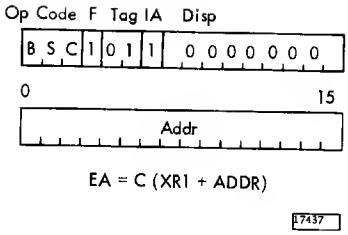
4. Shift Left and Count

A Shift Left and Count normalizes the A-register and leaves a remainder count in the index register. Note that four shifts have reduced the value in XR1 from 16 to 12. Also, regardless of the status of bit positions 8 and 9 in the index register, they are set to zero and bit positions 0-7 will be unchanged.



5. Branch or Skip on Condition

An indexed branch instruction with an indirect bit permits a unique branch to a table of addresses which contains an entry for each bit of the accumulator.



Indicator Identification

If the device requesting service is assigned to a DSW or PISW, it is necessary to determine which indicator in the DSW or PISW is responsible for the interrupt request. This identification can be made in an almost identical manner to the previously described program steps 1 through 8 of Figure 26:

1. An XIO Sense Device instruction is executed in step 5 instead of an XIO Sense Interrupt Level instruction. The area and/or modifier must specify the device or the status word.
2. The LDX instruction (step 6) loads the index register with the maximum number of indicators assigned to the DSW or the PISW instead of the number of interrupt request signals assigned to the ILSW.

NOTE: If only one device (one interrupt) is on an interrupt level, the program can be written so that only the DSW is sensed into the A-register and its indicators interrogated. Since only one interrupt is on the interrupt level, the ILSW need not be interrogated.

Industry, science, research, government – all are faced with the need for collecting increasing amounts of data within decreasing time scales. Physical measurements must be monitored and quantified with greater speed and accuracy than ever before. The collection of analog data and its conversion for presentation to the digital Processor-Controller is the function of the Analog Input features.

A physical phenomenon is first sensed and converted to an analog electrical signal by sensors or transducers, such as thermocouples or strain gages. Electrical signals from sensors or transducers may be in the millivolt, volt, or milliampere range. Low voltage signals (less than 1 volt) must be amplified to a level acceptable for conversion to digital form. All customer lines from transducers are terminated at the control system on screw-down terminals. The signals are also conditioned at the terminals, including the filtering of extraneous signals, known as noise.

Conversion of analog signals from a voltage level to digital information is accomplished by an Analog-to-Digital Converter (ADC). Such converters, however, are complex enough so that if multiple sources of analog signals are to be converted, they share the use of one ADC. The switching is accomplished by a multiplexer. The data path from sensor or transducer to processor is shown by Figure 28.

ANALOG INPUT UNITS AND FEATURES

The Analog Input Units and features provide modular packaged equipment used to convert voltage or current signals to digital values. The modules used to accomplish the conversions include analog-to-digital converters, multiplexers, amplifiers, and other signal conditioning equipment.

The units and features that accomplish the analog input function are briefly introduced below, followed by more detailed descriptions. A description of the operation of analog input and its relation to the P-C is given later in the Programmed Operation section.

As shown in Figure 29, customer input signals are routed through termination, signal conditioning elements, multiplexer switches, an amplifier (low level signals only), and into the analog-to-digital converter (ADC). The output of the ADC is presented to the P-C via the I/O control or the Data Channel from the ADC output register.

1851 Multiplexer Terminal – Model 1. A modular chassis which mounts in a rack enclosure; up to 64 analog input multiplexer points (2 wire), signal conditioning elements for each point, and up to two floating differential amplifiers can be mounted in each terminal.

1851 Multiplexer Terminal – Model 2. Similar to Model 1; however, thermocouples can also be directly connected and 62 multiplexer points are the maximum. A temperature measuring device is included in the terminal.

Multiplexer/R. A relay multiplexer to provide low level differential switching of analog input signals to allow use of a common amplifier and analog-to-digital converter. High level signals can also be handled. Up to 100 points per second switching rate can be attained.

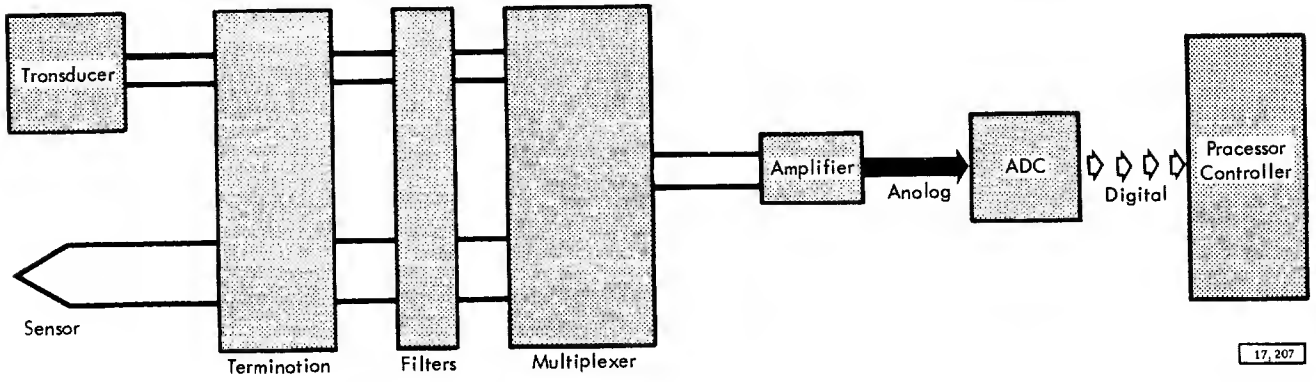


Figure 28. Data Path From Signal Source to P-C

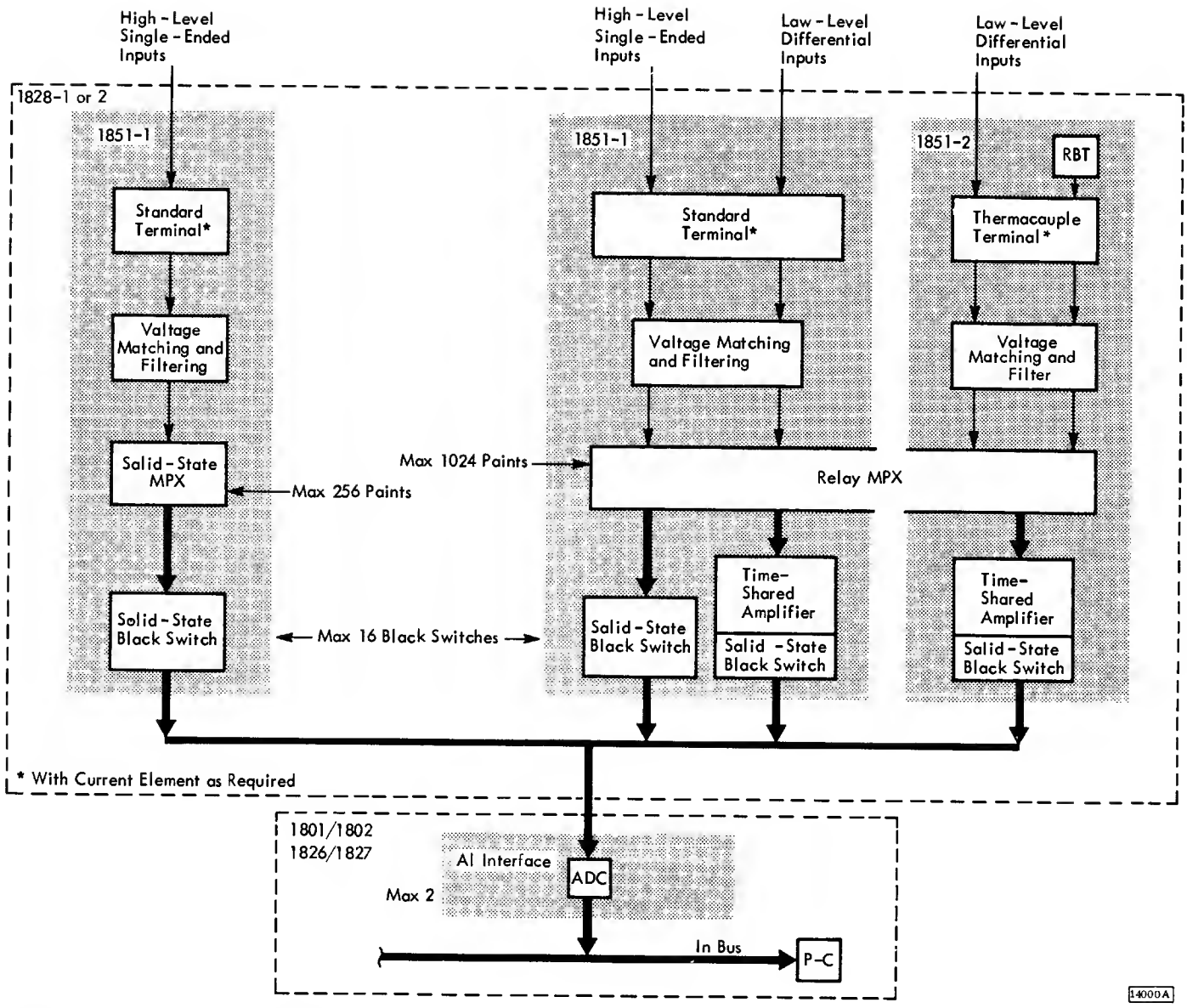


Figure 29. Interconnection of Analog Input Features

Multiplexer/S (HLSE). A solid state, high-level single-ended (HLSE) multiplexer to provide high-speed switching of analog inputs signals to allow use of a common analog-to-digital converter.

Multiplexer Overlap. This feature allows overlap of solid state and relay multiplexing.

Multiplexer/R Control and Multiplexer/R Control Additional. These features provide the necessary control circuitry to operate the Multiplexer/R points. Each feature can control up to 256 points.

Multiplexer/S Control. Control circuitry to operate the Multiplexer/S points is provided by this feature.

Signal Conditioning Elements. Five signal conditioning features are available:

1. CURRENT Element. 4-20 ma current input signals are converted into either 0.1-0.5 volt or a 1-5 volts.
2. FILTER Element. A low-pass, passive filter to reject common mode and normal mode AC noise.
3. VOLTAGE Element provides 2:1 voltage attenuation so that, for example, 100 millivolt signals may be read as 50 millivolt signals. With Multiplexer/R, this feature also provides the Filter Element function.
4. UNIVERSAL Element. A mounting facility for the Filter and Voltage Elements; or alternately

for custom signal conditioning with current, filter, voltage, and bridge capabilities – the components to perform the function are provided by RPQ* or the customer.

5. NO Element. Provides straight through coupling with no signal conditioning.

Floating Differential Amplifier. A time shared amplifier to raise each low level signal to the ±5 volt level of the ADC. Up to 256 Multiplexer/R points can use the same amplifier. It has one gain setting selected from: 500, 250, 100, 50, 25, and 10.

ADC – Model 1. Converts analog signals (±5 volt range) to digital values (8, 11, or 14 bits plus sign). This model provides a nominal 10 kc system conversion rate.

ADC – Model 2. Similar to ADC Model 1 but includes a Sample and Hold Amplifier for greatly increased system rates. The nominal system conversion rate is 20 kc for this model.

AI Data Channel Adapter – 1. Allows Chained Sequential mode of analog input (AI) operation by connecting a Data Channel to the analog input interface.

AI Data Channel Adapter – 2. Allows Random mode of analog input operation by connecting a second Data Channel to the analog input interface.

Comparator. Performs range checking on digital values developed by the ADC. The high and low limits are selectively obtained from the Processor-Controller for those values to be checked. When values are determined to be out-of-limit, then an interrupt informs the P-C. Only one P-C cycle is required for each value to be limit checked.

Analog Input Expander. Allows a complete analog input system to be configured around the 1826 Data Adapter Unit. Thus a second ADC or simply a separated ADC may be added to any 1800 System.

Multiplexer/R and Multiplexer/S Maximums and Ranges.

Although the maximum number of Multiplexer/R points and Multiplexer/S points are 1024 and 256, respectively, both maximums cannot be installed within the same system. The simultaneous maximums for each system are dependent upon the number of analog input ranges, as follows:

Multiplexer / R		Multiplexer / S
*Input Ranges Used	Maximum Points	Maximum Points
7	1024	144
6	1024	160
5	1024	176
4	1024	192
3	768	208
2	512	224
1	256	240
0	0	256

* Multiplexer /R input ranges are ± 10, ±20, ±50, ±100, ±200, and ± 500 millivolts for input to a differential amplifier, and ± 5.0 volts for direct input to the ADC. The only Multiplexer/S input range is ± 5.0 volts for direct input to the ADC.

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1851 MULTIPLEXER TERMINAL

The 1851 Multiplexer Terminal is a modular chassis in which multiplexing and signal conditioning features can be mounted. The 1851 terminals are mounted in a 1828 enclosure. Up to 19 terminals can be included for any one ADC in a system. Multiplexer/R and Multiplexer/S cannot be installed in the same 1851 terminal unit.

There are two models of the Multiplexer Terminal. The Model 1 provides for the insertion of up to 64 multiplexer points in groups of 16 points. Customer wires are terminated on screw down terminals. The Matching Elements are available for each Multiplexer Terminal. Up to two Differential Amplifiers can also be mounted in each terminal.

The Model 2 is a modified terminal to allow for thermal measurement of the terminals. Thus thermocouple wires can be directly connected to the terminals and the cold-junction temperature can be read by the P-C. The maximum capacity of the

*Request Price Quotation from IBM

Model 2 is 62 multiplexer points. One multiplexer address is used for the RBT (Resistance Bulb Thermometer) and another address is used for the power supply. These are the first two addresses that are installed in any 1851 Model 2. (Note: Therefore, the first Multiplexer/R group has only 14 analog input multiplexer points available for external source signals.) It is important that both an RBT reading and a power supply voltage reading be taken at intervals which are small compared with significant ambinent temperature change intervals. Separate readings are of course required for each Model 2 Multiplexer Terminal.

All other functions of the Model 2 Terminal are the same as the Model 1 Terminal. Thus nonthermocouple signals may be terminated in the Model 2.

MULTIPLEXER/R

The Multiplexer/R feature provides for relay multiplexing of high or low level analog inputs at a maximum speed of 100 points per second. The equipment is card mounted and plugs into the Multiplexer Terminal in groups of 16. For low level signals, up to 16 groups can be combined to form the input to one time-shared amplifier providing up to 256 input points per amplifier. Each amplifier has one fixed set gain, and the full scale input range for any group of Multiplexer/R points will be dependent on the gain of the amplifier to which it is connected. Gains available are: 500, 250, 100, 50, 25, and 10. High level inputs (0.5 to +5 volts) do not require an amplifier. Up to 256 high level points can be included in any ADC system.

The Multiplexer Overlap feature allows overlapping of switching times for the Multiplexer/R and Multiplexer/S (HLSE) points.

The Multiplexer/R can operate with a maximum of 200 volts common mode (DC or peak AC).

MULTIPLEXER/S (HLSE)

The Multiplexer/S feature provides for solid-state multiplexing of high-level, single-ended (HLSE) analog inputs. The settling time of this multiplexer is five microseconds. System speeds are dependent upon ADC, amplifier, etc., used in any particular system. The Multiplexer Overlap feature allows the overlapping of Multiplexer/R and Multiplexer/S within any single ADC on a system. Groups of Multiplexer/S are mounted in the Multiplexer Terminal-Model 1 and cannot be intermixed with Multiplexer/R points within a terminal.

The input voltage range is 0 to ±5 volts full scale. With the ADC Model 1, the multiplexer must be held on for the full period of conversion and the maximum duty cycle of any Multiplexer/S switch is 50%. Therefore the net result is to halve the rate at which conversions can occur. With the ADC Model 2 the multiplexer only stays on until the Sample and Hold Amplifier stores the analog voltage level. The multiplexer is then turned off. This allows less than a 50% duty cycle with the highest ADC conversion rates.

Multiplexer Overlap

A special feature is available which allows the two multiplexers, Multiplexer/R and Multiplexer/S, to be overlapped. There are three possibilities by which overlapping occurs. All three can be operative independently or at the same time.

1. Using the direct programmed control mode of operation, the selection of a point in the relay multiplexer may be started and then a series of conversions of solid state points may be performed while the relay point is being selected.

   When the relay multiplexing is complete, it obtains use of the ADC for conversion of the relay point. When the conversion of the signal at the point is completed and the resultant data in the ADC register is available, an interrupt is activated. Solid state and relay point interrupts are differentiated by programmed interrogation of the Solid State Multiplexer Busy indicator. If on, the interrupt is a solid state point; if off, a relay point.

   Relay point conversion has priority over solid state switching in the sense that an interrupt resulting from the completion of a relay point conversion will suspend the selection of a solid state point. The selection will not be completed until the converted relay point data has been read into core storage.
2. If a discrete conversion of a relay point is started under programmed control, a sequence of conversions of solid state points can be started on Data Channels. When the relay multiplexing is complete it obtains use of the ADC for conversion of the relay point. When the resultant converted data is available in the ADC register, an interrupt is activated. This is the normal "conversion complete" interrupt utilized for discrete conversions under programmed control. If the solid state conversions have not been completed when the relay multiplexer control captures the ADC, then the solid state conversions are continued as soon as the

ADC Register has been cleared. No further discrete conversion may be started until the solid state conversions are complete.

3. Under two Data Channel operations, overlapping is also possible. Relay addresses can be inserted in the data table of multiplexer addresses. These addresses will not have corresponding ADC values placed in the ADC converted data table. The relay point addresses are latched by the relay multiplexer control, and the interface control requests a further cycle to obtain the next solid statc multiplexer address from P-C memory. Random conversions proceed asynchronously until the relay multiplexer is ready. When the relay multiplexer is ready, the relay multiplexer control signals the ADC. The next point converted will be a relay point and an Interrupt will allow the P-C to transfer the value in the ADC Register to core storage under XIO-Read control, after which conversions are continued under Data Channel control. If another relay address is recognized before the first relay point has been converted, an interrupt occurs. This interrupt informs the P-C that a relay point was mislocated in the address table. The mislocated relay point will not be converted.

Efficient use of overlapping of relay and solid state multiplexing depends upon correct placement of addresses in the Multiplexer Address Data Table. Enough solid state multiplexer addresses must be included between relay addresses to insure that sufficient time is always taken so that the first relay point is converted and relay multiplexer control is ready.

Overlapping and Chained Sequential addressing are not compatible (See Programmed Operation section).

SIGNAL CONDITIONING ELEMENTS

Five signal conditioning features are integrally packaged with the multiplexer and terminals. The Filter, Current, and Voltage features serve the functions of normal mode filtering, current to voltage conversion and voltage range changing. The Universal feature allows custom filtering and voltage dividing in addition to bridges and other signal conditioning circuits; the components to provide this custom function are supplied by RPQ* or the customer.

*Request Price Quotation from IBM

The No Element feature provides straight through coupling with no signal conditioning.

Filter Element

The Filter Element feature provides low-pass passive filtering of the input signals for Multiplexer/R to reject both common mode and normal mode ac noise. Normal Mode Rejection of 125:1 60 cycle ac is provided. Maximum common mode rejection will be maintained with up to 3 samplings per second per point rates. The maximum safe voltage range is -0.5 to +6 volts.

A Filter Element cannot be installed on points for which Voltage Elements are ordered.

Current Element

The Current Element feature is used to translate a 4-20 ma current input into either a 0.1 - 0.5 volt or a 1-5 volt, voltage input. A precision resistor mounted across the appropriate pair of 1851 terminals performs this function; it may thus be used for single ended or differential inputs, and can be installed with Multiplexer/R or Multiplexer/S.

Voltage Element

This voltage divider input feature provides a 2:1 voltage attenuation with .01 ohm source impedance for one analog input signal (accomplished with a total resistance of 4K ohms). This allows, for example, the intermixing of 100 mv and 50 mv signals in the same Multiplexer/R group. Source impedances up to 1000 ohms can be accommodated, but recalibration will be necessary since the attenuation constant will be 2.5:1. The actual divider ratio varies with source impedance and can be calculated for any specific case so that a specific voltage divider can be supplied as an RPQ.

The Voltage Element with Multiplexer/R provides the same filtering function as the Filter Element.

Universal Element

The Universal Element feature is available to permit customer and RPQ controlled input networks to be installed in the Multiplexer Terminal. It is also the base upon which the Filter, Voltage and No Elements are mounted and is prerequisite for every multiplexer point used in the system.

No Element

This feature is simply a Universal Element wired for straight through coupling with no signal conditioning.

DIFFERENTIAL AMPLIFIER

This is a time-shared amplifier used in conjunction with the Multiplexer/R, to raise analog signals to the ADC input level of ±5 volts.

Any one gain setting selected from 500, 250, 100, 50, 25, and 10 can be specified. These allow input voltage ranges on the connected Multiplexer/R points to be: ±10, ±20, ±50, ±100, ±200, and ±500 millivolts.

A single amplifier can service up to 256 input points (16 blocks of 16 multiplexer relays). Up to two amplifiers can be mounted in one Multiplexer Terminal. Thus multiple amplifiers can be used for voltage range changing in place of using passive Voltage Elements.

ANALOG-DIGITAL CONVERTER (ADC)

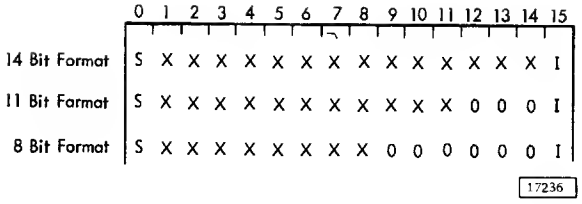
The ADC provides the 1800 with the ability to convert bipolar analog signals (±5 volt signal range) to digital values. Two models are available: Model 1 includes a buffer amplifier and has program selectable resolutions of 8, 11, and 14 bits. Model 2 is similar to the Model 1 except that it includes a sample and hold amplifier which provides for increased system speed of conversion.

The ADC conversion time is dependent only upon the number of bits of output that are to be developed. Conversion times are as follows: 8 bits, 29 μsec; 11 bits, 36 μsec; and 14 bits, 44 μsec. Therefore, ADC conversion rates are 23,000 to 35,000 conversions per second (not including amplifier settling time). The input impedances of the ADC Model 1 and Model 2 are 10 megohms and 0.1 megohms, respectively.

The 1800 System conversion rates will vary from 9,000 to 24,000 samples per second. (Dependent upon equipment installed and mode of operation.)

Data Word

The data word developed in the ADC Register is compatible with 1800 word format as shown below. Negative numbers are in 2's complement form and allow for 14 bits plus sign resolution. Conversion by the stored program of the value presented by the ADC should assume a position for the binary point. This position of the binary point does not change when the format (14, 11, or 8 bit) is changed, only the number of bits in the ADC converted value changes.



Notes:

1. S is the sign of the data: a zero bit is positive and a one bit is negative.
2. The X's indicate that a one or zero bit may appear to represent the converted value. With the 11 and 8 bit format the 0's indicate that only a zero will appear in these positions.
3. I is the overload indication bit. The presence of a bit indicates an overload condition; that is, the signal was outside the ±5 volts range.

14 BIT RESOLUTION EXAMPLE — BIT POSITIONS 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Normal Positive Binary Value	0 0 0 0 0 0 0 1 0 1 1 1 1 0 1 1 0
Decimal Equivalent	+187
Maximum Positive Value	0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0
Decimal Equivalent	+16382
Normal Negative Binary Value	1 1 1 1 1 1 1 0 1 0 0 0 1 0 1 0
Decimal Equivalent	-187
Maximum Negative Value	1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0
Decimal Equivalent	-16383
Positive Overload Condition	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Negative Overload Condition	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Note:

Decimal Equivalents Assume That The Binary Point Is Between Bits 14 And 15.

17 220

External Sync

The operation of the ADC can be controlled by an external timing (sync) pulse. When the Relay Multiplexer is used, a "ready" condition is transmitted to the external timing device after the Relay Multiplexer and block switches are settled. When the Solid-State Multiplexer is used, a

"ready" condition is transmitted before the solid-state switches are picked. The external device provides a sync pulse which allows the solid-state switches in either type multiplexer to pick and then conversion of the selected signal begins.

An "8" bit in the modifier of an IOCC, either "Write" or "Initialize Read," sets up the external sync mode. The absence of an "8" bit in the modifier of either a "Write" or "Initialize Read" command terminates the external sync mode.

External sync cannot be used during overlap (special feature) operations.

Buffer Amplifier

The Buffer Amplifier is a single-ended operational amplifier and is an integral part of the Model 1 ADC. The amplifier provides high-input-impedance (10 megohms) buffering of the ADC on a time-shared basis for those applications where it is unnecessary to provide a time-shared sample-and-hold input characteristic.

Sample-and-Hold Amplifier

The Sample-and-Hold Amplifier is an integral part of the Model 2 ADC; it is a single-ended amplifier capable of providing a short aperture time in the sampling of high-level analog signals and of providing a high accuracy hold function. The amplifier has an input impedance of 100K ohms. The P-C program must consider the reversed polarities obtained from sample-and-hold input points.

COMPARATOR

The Comparator performs selective checking on the digital values converted by the ADC. A range type check is made to confirm that the converted values are within specified limits. The limits are obtained from the Multiplexer Address Data Table (one P-C cycle delay allows both limits to be acquired) whenever a check is required. The P-C is informed of an out-of-limits condition by interrupt.

Operational Description

In order that a range comparison can be made, both a high limit and a low limit must be set. In converting many analog input source signals, it may be necessary to monitor each signal to assure that they remain within specified bounds. Normally, a number of these signals are redundant and other signals need only be checked occasionally. To allow for flexibility of checking input signals, limit words (a P-C word containing both the high and low limit) can be generated for each input signal that is to be checked. A separate control is added to instruct the Comparator to perform checking.

It should be noted that limit words need not remain static. For example, when a particular limit is exceeded, then a single change will permit recognition of the return of the signal within the former limits. The high limit is substituted for the low limit and the maximum value is set for the high limit. If the interval timer is read after each limit is exceeded, then the time interval that the signal was out-of-limits is known.

Limit Words

The high and low limits are stored in P-C storage within the Multiplexer Address Data Table (see Figure 30). These limit values are expressed in eight bits (seven bits plus sign) with negative numbers represented in two's complement form. The Comparator is only used under the Random Mode of Operation (See Programmed Operation section). Following each Multiplexer Address entry that is to be checked is a limit word. The Multiplexer Address entry contains two control bits in addition to the analog input point address. These bits are stored in positions one and two of the multiplexer address word. The L bit, stored in position one, indicates the presence of a limit word as the next word in memory. The K bit, stored in position two, indicates whether or not a comparison is to be performed. In addition, bit position three (Q) indicates Multiplexer/S (1-bit) or Multiplexer/R (0-bit).

Figure 30 shows a sample table. The word count to control a two Data Channel operation is obtained from the Data Table which receives the converted values. Only the scan control bits are used from this table to provide unique chaining. Note that if the Multiplexer Overlap feature is installed, a limit word cannot follow Multiplexer/R addresses.

Comparison Cycle

At the initiation of a conversion cycle, the multiplexer address is placed in the Analog Multiplexer Address Register; then a conversion is started. If a comparison is to be made, a limit word is placed in the Comparator Register. When conversion is complete, comparison proceeds with whatever value is in the 8 high-order bits of the ADC Register. If the converted value falls between

the limits in the Comparator Register, the next multiplexer address is brought in from the P-C.

If an out-of-limits condition is detected, the bits identifying the multiplexer point and the type of condition are saved in the comparator. An interrupt unique to the Comparator is activated to alert the P-C and further comparisons are suppressed until the stored identification word is read into the P-C with an XIO Sense instruction. The out-of-limit conditions are:

High out-of-limit (ADC > High Limit)
Low out-of-limit (ADC < Low Limit)

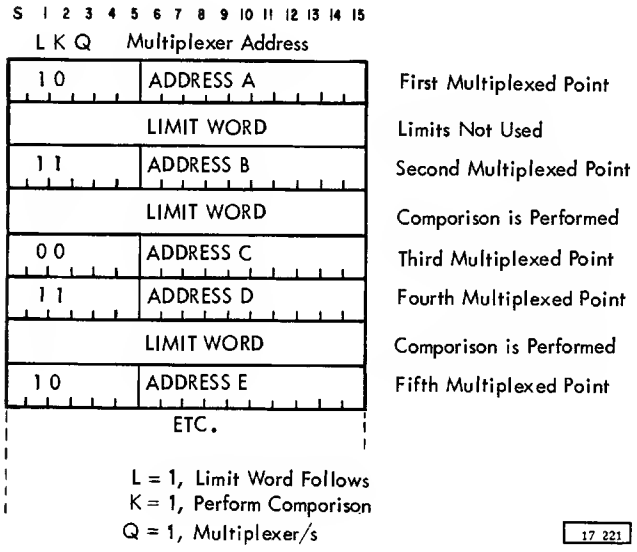


Figure 30. Data Table with Limit Words

ANALOG INPUT EXPANDER

This feature provides two principal advantages:

1. It doubles the capacity of the analog input features.
2. It allows the analog input features to be structured separate from the Processor-Controller.

The Analog Input Expander is a feature of the 1826 Data Adapter Unit, which provides the basic capability for attachment of an ADC, Comparator, Multiplexer Terminals, etc. This second analog input system attaches to I/O Control and Data Channels in a manner similar to the first analog input system. Thus the system conversion rates can be doubled, neglecting I/O interaction.

PROGRAMMED OPERATION

This section describes the control modes that are available for the slection of analog input points, conversion of the selected analog signal to a digital value, and then the transfer of the digital value to the P-C.

There are three basic control modes for the input of analog data: (1) Programmed, (2) Chained Sequential, and (3) Random. They are described in detail below. Essentially the Programmed mode requires the execution of at least one XIO instruction (see I/O Control) for each value that is read into the P-C. The Chained Sequential mode uses one Data Channel and allows any number of groups of sequentially addressed values to be read into the P-C with the execution of one instruction (XIO). Sequentially addressed values are those which are developed from multiplexer addresses in sequence. That is, values with multiplexer addresses 23, 24, ... 46 would constitute a sequential group of 24 points.

The Random mode uses two Data Channels and allows each point to be addressed uniquely. Any number of groups of points may be addressed, converted, and read into the P-C with the execution of two XIO instructions.

Programmed Control

Using the Direct Program Control (DPC) mode of operation, two Execute Input/Output (XIO) instructions are used. The first instruction, an XIO Write, addresses the multiplexer and selects the analog input point which is to be converted. Upon completion of multiplexing, an internal signal is sent to the ADC to start the point conversion. When the ADC has completed the conversion, an interrupt signal is sent from the ADC to the P-C. The P-C initiates a subroutine (for interrupt description, see Interrupt section) to determine the cause of interrupt, if necessary, and provides the second instruction, an XIO Read, to transfer the data to storage. This mode of converting data from analog signal to digital value in storage is a discrete addressing method; that is, two instructions result in the acquisition of data from one input point.

Sequential Programmed Control. A standard operation requires the execution of only one XIO Write instruction for many XIO Read instructions if the subsequent analog input points to be converted are in sequence. A bit in position 8 of the IOCC addressed by the XIO Read instructs the multiplexer to increment by one the address previously converted

and then to perform the next cycle. A cycle here is composed of selecting the analog input point, converting the selected analog signal, and initiating an interrupt to inform the P-C that the converted value is in the ADC register ready to be read into P-C storage. The absence of a bit in position 8 of a Read IOCC terminates the operation.

Chained Sequential Control

Using a single Data Channel, a sequence of analog inputs can be scanned, converted, and stored in core storage with one XIO instruction to initiate the action. The two word IOCC contains the core storage address where the Scan Control bits and the Word Count are stored for the operation. The Word Count sets up the number of input signals to be converted in the sequence. The Scan Control bits determine if an interrupt is given and whether or not chaining or termination of the operation will be effected when the Word Count reaches zero.

The Word Count is in the first word of the Data Table (Figure 31). Note that the Word Count precedes the multiplexer address word which is at location 3000 in this example. The Data Channel "writes" this word to the Analog Multiplexer Address Register (AMAR) which initiates the selection of analog points and conversion to digital values. At the completion of each conversion the converted data is read into sequential storage locations. After each transfer of data, the Word Count is decremented by one and the previous address in the AMAR is incremented by one. The new address causes the next sequential point to be selected. This operation continues until the Word Count reaches zero.

Figure 31 illustrates a table in core storage which could be used for Chained Sequential Operation. The IOCC word that initiates this analog input function is located in storage locations 3042 and 3043, which are at the end of the second table in this example. The IOCC initializes the multiplexer and the ADC and then places the address of the Word Count (the first word in the table) in the Channel Address Register (CAR) of the Data Channel. In this example, the Word Count is located in storage location 2999.

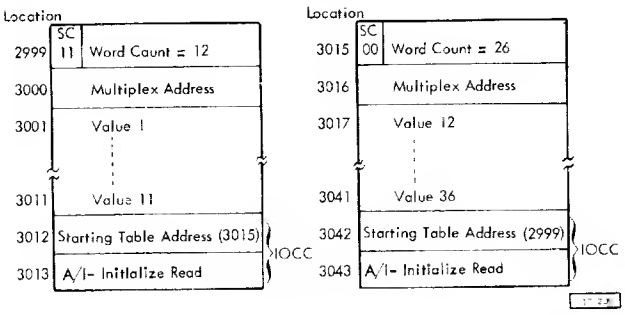


Figure 31. Data Table, Chained Sequential Control

The ADC now requests a cycle to place the word count into the Word Count Register (WCR). In this example the word count is 12. CAR is incremented by one so that now CAR contains the address 3000. On the next cycle the initial multiplexer address is transferred from location 3000 to the AMAR. When multiplexing is complete, a signal is sent to the ADC to start conversion. At the completion of conversion, the ADC register contains a digital value and a cycle request is made. CAR (now containing address 3001) addresses memory and the digital value in the ADC output register is transmitted to location 3001.

The above procedure is repeated and continues until the WCR reaches zero. At this time, the Scan Control bits are monitored and it is discovered that they indicate continued scanning (11). The next table address (3015) is loaded into CAR. This table address is the location of the Word Count and Scan Control bits for the next sequence of input signals. (The second word of this IOCC is not used in this example and would only be used if at some point an XIO instruction referenced location 3012.) When the WCR again reaches zero, the Scan Control bits now indicate that the operation is to be terminated (00 also indicates an interrupt). The operation is terminated and a new XIO instruction is required to initiate further operation of the analog input system.

Random Control

In this mode of operation, the multiplexer addresses are transmitted on one Data Channel and the ADC data is transmitted on a second Data Channel. The operation is initiated with two XIO instructions. The first instruction sets up the controls for transferring converted data from the ADC to storage on one channel and loads the Scanning Control Register (SCR) and the Word Count Register (WCR) for the operation. The Word Count is equal to the number of converted values to be stored.

The second instruction references the first multiplexer address and initiates the transfer of all data table addresses from P-C storage to the multiplexer on the other channel.

When the first analog input point has been selected, a start impulse is given to the ADC. At the completion of the first conversion, a memory cycle transfers the converted data to the set up Data Table in the P-C. Alternate P-C cycle requests bring in the multiplexer addresses on one channel and transfer the converted data to storage on the other channel. This operation continues until the

WCR is decremented to zero. When the WCR reaches zero, the Scan Control bits are interrogated to determine if an interrupt is to be given and whether the operation is to continue or terminate.

Figures 32 and 33 illustrate the multiplexer address and ADC storage tables to perform a random addressing operation. An XIO instruction referencing location 3522 would initiate ADC action. Another XIO instruction referencing location 3120 initiates multiplexing.

In this example (Figures 32 and 33), 120 points are being read and converted in a random sequence. The two ADC tables are chained together while the multiplexer table is chained to itself. The Scan Control bits cause an interruption at the end of each ADC table. The number of multiplexing addresses set up in the Multiplexer Address table must equal the word count set up in the ADC table.

Systems with two Data Channels may convert values using any mode. The mode is selected by appropriate bits in the Function or Modifier of the IOCC. In the Chained Sequential Mode (with two Data Channels) the Data Channel used by the Multiplexer is not used, and the operation is the same as that previously described under Chained Sequential Order.

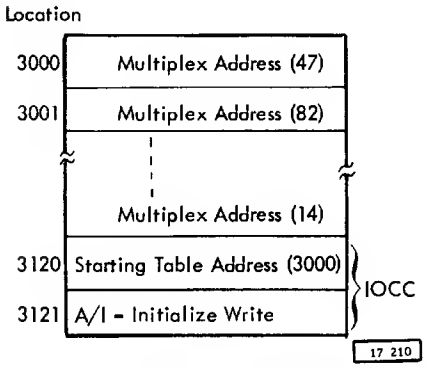


Figure 32. Multiplexer Address Table, Random Addressing

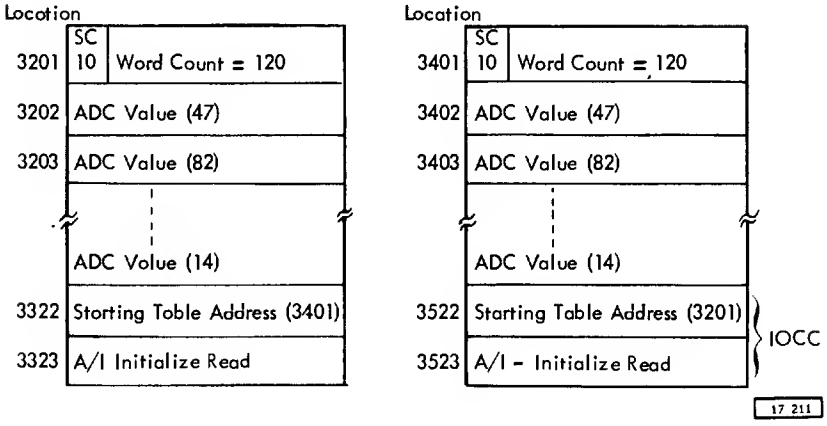
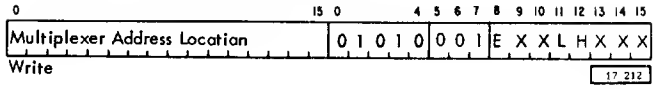
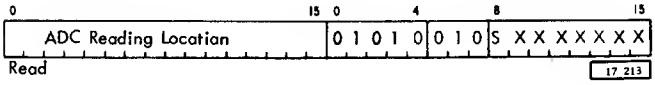


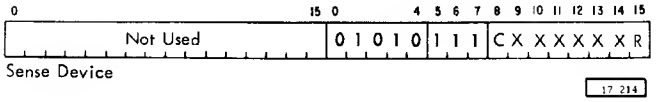
Figure 33. ADC Storage Tables, Random Addressing

I/O CONTROL COMMANDS - ANALOG INPUT

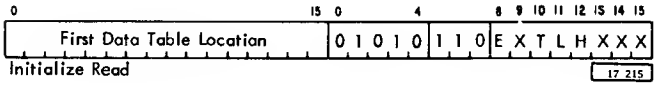
DIRECT PROGRAM CONTROL

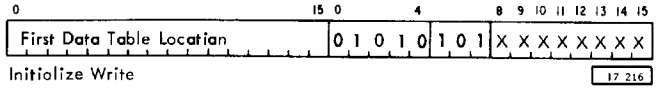






DATA CHANNEL



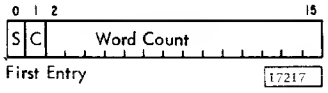


where:

01010	is the assigned Area for Analog Input.
X	is not used.
C	one bit specifies Comparator status word; no bit Analog Input status word.
E	one bit means External Synchronized.
L	one bit specifies Low Resolution – 8 bit plus sign.
H	one bit specifies High Resolution – 14 bit plus sign.
R	one bit resets indicators.
S	one bit specifies Sequential Programmed Mode.
T	one bit specifies Two Data Channel Operation, Random Mode.

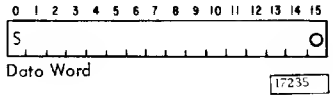
NOTE: No L and H bit specifies 11 bit resolution.

Data Table Formats



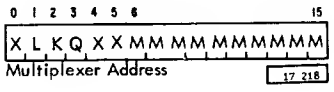
where SC are the Scan Control Bits

S	One bit causes chaining to occur
C	No bit causes interrupt at end of Table



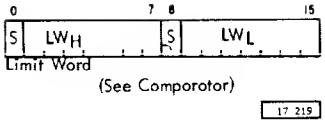
where:

S	Sign bit
O	One bit indicates Overload



where:

X	Means not used
K	Perform Comparison (see Comparator)
L	One bit means Limit Word follows (see Comparator)
Q	One bit signifies Solid State Multiplexer; No bit, Relay Multiplexer.
M-M	Multiplexer Address



where:

S	is the sign bit
LW_L	is the Low Limit
LW_H	is the High Limit

Device Status Format

The execution of an XIO Sense Device instruction with the area code specifying Analog Input (01010) will cause the Device Status Word to be read into the accumulator. The bits of the Device Status Word are:

	0	WORD COUNT EQUALS ZERO.
	1	DPC SOLID STATE (SS) MULTIPLEXER POINT CONVERSION COMPLETE.
	2	DPC RELAY MULTIPLEXER POINT CONVERSION COMPLETE.
*	3	STORAGE PROTECT VIOLATION.
	4	PARITY CONTROL ERROR.
	5	PARITY DATA ERROR.
	6	ADC OVERLOAD.
	7	OVERLAP CONFLICT.
	8	DATA CHANNEL, SS MULTIPLEXER, OR AMAR BUSY.
	9	DPC RELAY MULTIPLEXER BUSY.
	10-14	NOT USED
	15	ANY ERROR (turned on by any one of bit positions 3, 4, 5, 6, or 7).

With a Comparator (interrupt level assigned to the Comparator appears in Modifier bits of IOCC) an additional Device Status Word will be:

*Causes Interrupt

	Bit	Significance of One Bit
*Interrupt	0	High out-of-limit
	1	Low out-of-limit
	2	Overload
	3	Solid State Multiplexer
	4, 5	Not used
	6 ... 15	Multiplexer Point Address

Note: Bit 2-Overload is common to both of the above Device Status Words. That is, if the interrupts of the two Device Status Words are assigned to different interrupt levels, then Overload will cause both levels to interrupt.

Analog Input Indicators

End of Table. Turned on and causes an interrupt when: (1) the end of a table is reached during a Data Channel operation, and (2) the Scan Control bits have specified an interrupt at the end of table. The End of Table indicator is reset when sensed if bit 15 in the Sense Device instruction is "on."

DPC SS Conversion Complete. Turned on and causes an interrupt in a Direct Program Control (DPC) operation when a Solid State (SS) Multiplexer point conversion is complete and the converted data is ready to be transferred to core storage.

DPC Relay Conversion Complete. Turned on and causes an interrupt in a DPC operation when a Relay Multiplexer point conversion is complete and the converted data is ready to be transferred to core storage.

Storage Protect Violation. Turned on and causes an interrupt when the program tries to store converted ADC data into a "read only" core storage location. Analog input operations are halted.

Parity Control Error. Turned on and causes an interrupt when a parity error is detected in control commands and words. Analog input operations are halted.

Parity Data Error. Turned on and causes an interrupt if a parity error is detected when multiplex address or converted data are transmitted between the P-C and analog input interface.

ADC Overload. Turned on and causes an interrupt when input to the ADC exceeds the range of the ADC and the Comparator is not used (see Comparator Overload).

Overlap Conflict. Turned on and causes an interrupt when a second relay point is addressed before the first relay point has been converted during a two data channel overlap operation.

CS, SS, or ADC Busy. Turned on when the SS Multiplexer is addressed, or during a DC operation (relay or SS), or when the ADC is busy. The indicator is turned off when the word count equals zero with no chaining, or a DPC solid state conversion is completed, or the ADC is no longer busy. No new instruction can be initiated except Sense Interrupt Level, Sense Device, or Control when this indicator is on.

DPC Relay Busy. Turned on when a Relay Multiplexer is addressed by a Write function, or when a Relay Multiplexer is sequenced by the sequence bit in the modifier of a Read function. The indicator is turned off 1.5 milliseconds after the relay conversion is complete. A new relay point can be initiated after the DPC Relay Conversion Complete interrupt has been serviced. However, AMAR (ADC) Busy will be on for the 1.5 milliseconds. The SS Multiplexer can be used with the Overlap feature when this indicator is on.

High Out-of-Limit. Turned on and causes an interrupt when the Comparator indicates an ADC reading above limits.

Low Out-of-Limit. Turned on and causes an interrupt when the Comparator indicates an ADC reading below limits.

Overload (Comparator). Turned on during a compare operation if the input to the ADC exceeds its range.

*All interrupts must be assigned to the same interrupt level. The High and Low out-of-limit conditions are always combined into one interrupt signal.

ANALOG INPUT EXECUTION TIMES

The following are typical times required for reading a series of analog input points. Note that times are shown for both core storage cycle times, 2 and 4 μsec. ADC conversion time is for 14-bit resolution. Eleven or 8-bit resolution is 8 and 15 μsec per point faster, respectively. The Comparator has no appreciable effect (one core storage cycle) on these times unless an out-of-limit occurs. No time is included for whatever program housekeeping may be necessary.

DIRECT PROGRAM CONTROL OPERATIONS

Multiplexer/R – ADC Model 1

Per Point	2 μsec	4 μsec
XIO Write	.010 ms	.020 ms
MPLX Relay	9.700	9.700
ADC Conversion	.044	.044
Interrupt	.110	.220
XIO Read	.010	.020
	9.874 ms	10.004 ms

Multiplexer/S (HLSE) – ADC Model 1

Per Point	2 μsec	4 μsec
XIO Write	10 μsec	20 μsec
SS MPLX and Buffer Amplifier	8	8
ADC Conversion	44	44
Interrupt	110	220
XIO Read	10	20
	182 μsec	312 μsec

Multiplexer/S (HLSE) – ADC Model 2

Per Point	2 μsec	4 μsec
XIO Write	10 μsec	20 μsec
SS MPLX and S & H Amplifier	8	8
ADC Conversion	44	44
Interrupt	110	220
XIO Read	10	20
	182 μsec	312 μsec

DATA CHANNEL OPERATIONS

One DC – MPLX/S – ADC Model 1

Initialize	2 μsec	4 μsec
XIO Iniitalize Read	8 μscc	16 μsec
Cycle Steal (CS) Word Count	4	8
CS Initialize MPLX ADDR	2	4
	14 μsec	28 μsec

Per Point		
SS MPLX and Buffer Amplifier	8 μsec	8 μsec
ADC Conversion	44	44
Wait	43	43
CS Read Data	2.5	5
	97.5 μsec	100 μsec

Chaining		
CS New ADDR	2 μsec	4 μsec
CS Word Count	2	4
CS MPLX ADDR	2	4
	6 μsec	12 μsec

One DC – MPLX/S – ADC Model 2

Initialize and Chaining times are the same as those for the preceding One DC – MPLX/S – ADC Model 1 times.

Per Point		
SS MPLX and S & H Amplifier	12	12
ADC Conversion	44	44
CS Read Data	2.5	5
	58.5 μsec	61 μsec

Two DC's – MPLX/S – ADC Model 1

Initialize

XIO Initialize Read	8 μsec	16 μsec
XIO Initialize Write	8	16
CS Word Count	2	4
CS MPLX ADDR	2	4
	20 μsec	40 μsec

Per Point

SS MPLX and Buffer Amplifier	8 μsec	8 μsec
ADC Conversion	44	44
Wait	43	43
CS Read Data	2.5	5
	97.5 μsec	100 μsec

Chaining

CS New ADDR	2 μsec	4 μsec
CS New ADDR	2	4
CS Word Count	2	4
CS MPLX ADDR	2	4
	8 μsec	16 μsec

Two DC's –MPLX/S – ADC Model 2

Initialize and Chaining times are the same as those for the preceding Two DC's – MPLX/S – ADC Model 1 times.

Per Point

SS MPLX/S and S & H Amplifier	12 μsec	12 μsec
ADC Conversion	44	44
CS Read Data	2.5	5
CS MPLX ADDR	2	4
	60.5 μsec	65 μsec

THERMOCOUPLE PROGRAMMING

A thermocouple is a temperature-measuring device. It provides an analog voltage which is developed by the difference between the ambient temperatures of the thermocouple measuring junction and the thermocouple block reference junction. A resistance bulb thermometer (RBT) and its associated circuit components are mounted on the block to measure the reference temperature. The RBT circuit also provides a reference voltage signal (V_R). The 1800 uses the thermocouple, RBT, and V_R signals to compute the measured temperature.

Measuring Thermocouple Temperatures with the 1800

The 1800 is connected to each process thermocouple via the 1851 Model 2 Multiplexer Terminal. The thermocouple measuring junction is located in the process area where temperature sensing is desired, and the reference junction is located on the 1851 Model 2 terminal block. The reference junction wires are extended to a matching card in the 1851. The 1800 monitors reference temperature fluctuations by means of an RBT, located on each thermocouple terminating block for reference-temperature sensing, and corrects for these fluctuations through calculations performed as part of the program.

Resistance Bulb Thermometer (RBT)

Essentially, an RBT is a wire-wound resistor whose electrical resistance varies with temperature. The resistor is electrically connected to a Wheatstone bridge (balanced circuit). A temperature variation causes a change in resistance and a consequent unbalance of the bridge circuit. The RBT circuit provides two signals for 1800 program evaluation; the voltage produced by the RBT, and an RBT reference voltage. Thus, not only are thermocouple signals compensated for by reference temperature fluctuations, but the reference temperature signal itself is read by the computer to permit compensation for any RBT supply voltage variations that may occur.

Thermocouple Programming and Conversion

The conversion of a thermocouple signal to a meaningful and accurate temperature value is performed as part of the computer program. The signals from the thermocouple and the RBT circuit, plus related thermocouple and RBT data, provide the means for mathematical analysis and conversion. Thermocouple data is available from commercial sources for each thermocouple type, i.e., tables and curves which express the temperature-to-millivolt relationship. Data for the RBT supplied with the thermocouple terminal block is provided below. Three points should be stressed about the conversion procedure which follows: (1) It is recognized that there are

other means, such as curve fitting, to convert thermocouple signals, (2) The procedure below is valid only where the RBT supplied with the thermocouple terminal block is used, and (3) This procedure pertains to the signal conversion of only one thermocouple type, i.e., constants A, B, C, and D (see below) must bc computed and stored for each thermocouple type:

1. Study the thermocouple temperature-to-millivolt curve and determine the number of segments or divisions that must be made to obtain the desired degree of accuracy. For example, the iron-constantan thermocouple curve shown in Figure 33.1 covers a temperature range of -50° to +850° C. This range may be divided into nine segments as follows: -50° to +50°, 50° to 150°, 150° to 250°, 250° to 350°, 350° to 450°, 450° to 550°, 550° to 650°, 650° to 750°, and 750° to 850°C.

   This segmentation is required because thermocouple millivolt output is not a straight line relationship with respect to measured temperature, particularly at the upper end of the thermocouple temperature range. Smaller segments, of course, provide a more linear or straight line approximation.
2. Take the upper and lower millivolt valucs from each segment, and use the ADC-per-millivolt values given in Table 7.1 to obtain equivalent ADC values for the upper and lower millivolt values of the segment. For example, a 15-millivolt signal is converted to an ADC value of 15 x 327.6 or 4914.0, where the signal range is ±50 millivolts and the ADC resolution is 14 bits. Since all thermocouple signals are converted to digital values, the use of ADC values rather than millivolt values facilitates the computation of actual temperatures.

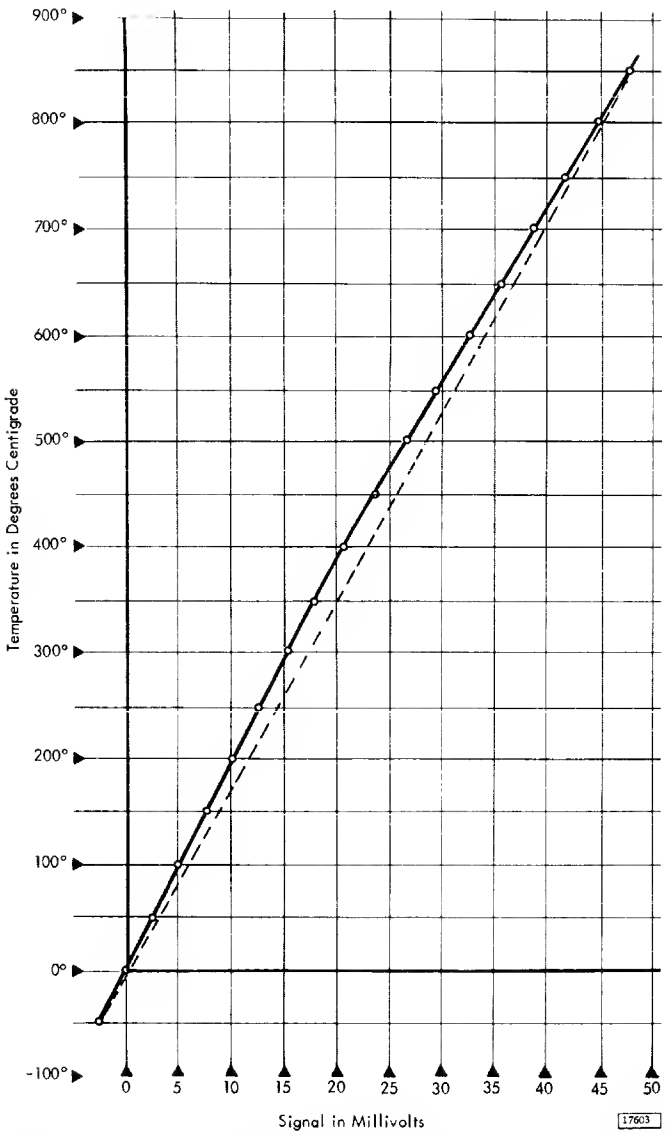


Figure 33.1. Iron-Constantan Thermocouple for -50 C to +850 C Range

Table 7.1 ADC Values Per Millivolt Shown in Shaded Area

Signal Input Range	ADC Resolution		
	14 Bit	11 Bit	8 Bit
±10 mv*	1638.3	1637.6	1632.0
±20 mv*	819.1	818.8	816.0
±50 mv*	327.6	327.5	326.4
± 100mv	163.83	163.83	163.20
± 200mv	81.91	81.88	81.60
± 500mv	32.76	32.75	32.64

* Only 10, 20, 50 millivolt ranges may be terminated on first 16 positions of thermocouple block. 17604

3. For each segment, use the formula

   temperature = A (ADC) + B

   twice to solve for A and B, the two unknowns, i.e., once using the upper temperature and corresponding ADC value and once for the lower temperature and corresponding ADC value. A is in degrees per digit. B is in degrees centigrade. Actually, A is the slope of the segment and B is in the intersection of the segment if extended to the y-axis of the thermocouple curve.
4. Store A and B for each segment.

5. Use the same formula (step 3) to solve for A and B in the temperature area of 25° C, which is the normal temperature region for the RBT (approximate room temperature). Use these A and B values in the following formulas

$$C = \frac{1}{A} \qquad D = -\frac{B}{A}$$

These formulas express the thermocouple block RBT relationship to the thermocouple signal; C and D are used for the linear conversion from temperature to ADC value of the computed RBT temperature (step 8). C is a digits per degree value, and D is a digit value.

6. Store C and D. You now have stored: (1) a pair of constants, A and B, for each segment of the curve, and (2) constants C and D for the base temperature of the RBT.

In the equations which follow:

T_{rbt} = RBT temperature

V_{rbt} = ADC value for RBT signal

V_r = ADC value for RBT reference voltage signal

R_{rbt} = corrected ADC value for T_{rbt}

V_{tc} = ADC value for thermocouple signal

R_{tc} = adjusted ADC value for V_{tc}

T_{tc} = thermocouple temperature

7. Read both signals of the RBT circuit and use their ADC values in the formula

$$T_{rbt} = 28.82 \frac{V_{rbt}}{V_r} + 5.0$$

to solve for the "RBT temperature (T_{rbt})." V_{rbt} and V_r are the ADC values obtained by reading the RBT signal and the RBT reference voltage signal (the first two addresses on the thermocouple block). The values, 28.82 and 5 (expressed in degrees centigrade), are constants for the RBT supplied with the thermocouple block. These values must be converted to degrees Fahrenheit if the thermocouple tables and curves are expressed as such (F = 9/5 (C) + 32).

8. Use the formula

$$R_{rbt} = C\left(T_{rbt}\right) + D$$

to obtain a "corrected ADC value for the RBT (R_{rbt})." C and D were obtained in step 5; T_{rbt} was obtained in step 7.

9. Read the thermocouple signal, and use its ADC value in the formula

$$R_{tc} = V_{tc} + R_{rbt}$$

to obtain an "adjusted ADC value (R_{tc})."

10. Use the formula

$$T_{tc} = A\left(R_{tc}\right) + B$$

to compute the actual thermocouple temperature (T_{tc}). A and B are selected according to the ADC value of R_{tc}, i.e., whatever segment the value of R_{tc} falls into, the A and B values are used from that segment.

Example of Thermocouple Conversion

Example: An iron-constantan (type J) thermocouple is installed in a temperature region of 800° C. The signal range of the thermocouple is ±50 mv and the ADC resolution is 14 bits. The A and B values for the segment that includes 800° C are: A = .04762, B = 90.00. The A and B values for the segment that includes 25° C are: A = .0609, B = -1.5.

From step 5: C = 16.4 and D = 24.6

Assume the RBT temperature (T_{rbt}) is 25° C; then from step 8:

$$R_{rbt} = 410.25$$

Assume the ADC value of the thermocouple is 15132:

$$R_{tc} = 15542.25$$

and from step 10:

$$T_{tc} = 830.1°C$$

DIGITAL INPUT

These features enable the Processor-Controller of the 1800 to accept real-time digital information in a digital format. The modular design of the feature permits individual system tailoring as to type and quantity of digital input data, such as:

Contact Sense	Mechanical Counters
Voltage Level Sense	Electronic Counters
Contact Interrupt	Rotary Switches from operator
Voltage Level Interrupt	Sense Switches from operator
Digital Voltmeters	Pulse Tachometers
Special Analog-to-Digital Converters	Frequency Meters
Turbine Flowmeters	Watt-Hour Meters
Shaft Encoders	Vibration Detectors
Electronic Register e.g., Telemetry	Weighing Devices

Digital Input is brought into the system in 16-bit groups. The format may be in any form. For example:

Unrelated bits from Contact or Voltage levels
Binary numbers
Binary-coded-decimal digits
Decimal digits
Gray code digits

Any mixture of digital formats can be handled. Conversion from one base to another can be easily and quickly implemented by the P-C. Data input is via Direct Program Control or a Data Channel. One instruction is used in Direct Program Control to bring 16 bits of data into core storage. Where a Data Channel is used, one instruction initiates a cycle stealing operation that brings many 16-bit groups of data into core storage (one group per memory cycle). The number of groups read — sequentially, randomly, or single address — as well as synchronization of the P-C to the input data is handled automatically.

Interrupt conditions from the process are brought into the P-C in 16-bit groups, with up to four priority levels of interrupt and four interrupt conditions per level for each 16-bit group.

High-speed 8-bit binary electronic pulse counters are available as a special feature. Two of these counters may be coupled together to form a 16-bit binary counter. Counters are read into core storage as digital input groups, 16 bits at a time.

As shown in Figure 34 the combined capacity of the Digital Input and Pulse Counter features is 1024 bits, as follows:

Digital Input
8 adapters x 8 Digital Input groups
x 16 bits per group = 1024

Pulse Counter
8 adapters x 16 Pulse Counters
x 8 bits per counter = 1024

Any combination of the above may be used within the capacity of 1024 bits.

The capacity of the Process Interrupt feature is 24 priority levels or 384 bits, as follows:

8 adapters x 3 Process Interrupt groups
(24 levels)
x 16 bits per group = 384

DIGITAL INPUT UNITS AND FEATURES

The following units and features may be added to the system to provide Digital Input functions:

1826 DATA ADAPTER UNIT

This unit provides housing expansion of Digital Input and Digital Output points. There are two models: Model 1 is free standing, externally connected by cable. Model 2 is directly connected to a Model 1 or the Processor-Controller. Several Model 2's may be connected together. The following features are available for the 1801, 1802, and/or 1826.

Digital Input Adapter

Prerequisite feature for Digital Input (Contact), Digital Input (Voltage) and High-Speed Digital Input. Each of these provides for 128 bits of digital input. (Maximum - eight per system)

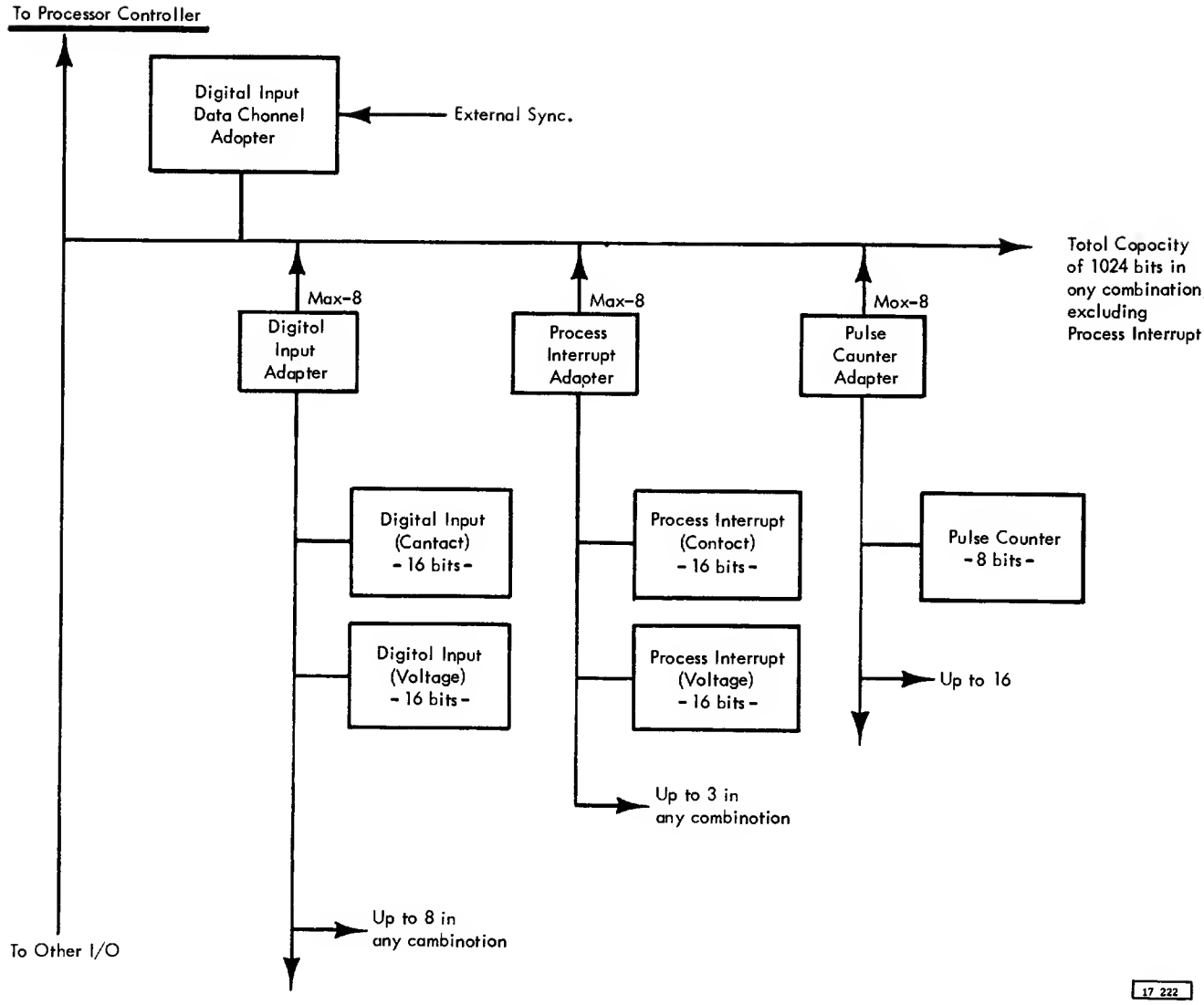


Figure 34. Digital Input Schematic

DIGITAL INPUT

Digital input in 16-bit groups can be handled. Any logical grouping of 16 bits can constitute a Digital Input group. For example:

16 bits of status information
4 4-bit BCD digits
1 10-bit coded decimal digit and 6 bits of status
1 16-bit binary number

Two types of Digital Input bits can be terminated in groups of 16. One type operates in conjunction with a customer supplied process contact. The second type senses the level of a voltage supplied from the customer's equipment.

Screw-down type terminations are provided to terminate the customer's input wires. Input groups of 16 bits are available to a total of 64 groups. Data is brought in on two wires per bit. An input channel, 16 bits wide, for special consoles and other low speed devices can be achieved by selection of devices onto the channel via the Digital Output features.

An XIO command received by the Digital Input feature contains the address of a Digital Input group and selects the group to be read into core memory or the Accumulator. Modifier addresses of 64_{10} through 127_{10} are assigned by the customer. If a process contact is closed or the voltage level is positive, a one bit will be placed in the designated bit position of that word. An open contact or negative level will result in a 0 bit being sent. The first sense bit is located in bit position zero, the second

in bit position one, etc., to the 16th bit in bit position 15 of the word. The Read function of the XIO instruction brings the addressed group into a core storage word and the Sense function brings the addressed group into the A-register (Accumulator). The Sense function is also used to read the digital input status word into the Accumulator. The status word contains the indicators for Digital Input.

Digital Input (Contact)

16 contacts* per group
Binary one-contact closed
Binary zero- contact open
Twisted pair customer input wires are recommended.
(Two Wire, screw down, termination)
Maximum total loop resistance — 1,000 ohms
Minimum open circuit resistance — 50,000 ohms (line to line or line to ground)
(Maximum Shunt Capacitance — (total between lines) - 0.5 μf
Maximum Series Capacitance — (total of loop including suppression) — 10 millihenries
Read speeds up to 500,000 words/sec are possible in burst mode when Data Channel feature is present with 2 μsec memory, but repetitive reading of the same group should be conditioned by the following:
Delay following process contact closure before reliable sense condition is eatablished — 4 msec maximum
Delay following process contact opening before reliable sense condition is established — 6 msec nominal, 10 msec maximum.

Adequate protection has been incorporated in this feature to prevent permanent damage to IBM equipment if 120 vac is accidentally connected to a pair of customer input terminals.

Digital Input (Voltage)

16 voltage levels per group
Two wire, screw down, termination
Line lengths and resistances can be of any magnitude provided that the dc voltage levels appear within tolerances at the screw down terminals. Twisted pair wires are recommended.
The voltage levels are:

Binary One: -1 v min to +30 v max
Binary Zero: -6 v min to -30 v max

*Contact must be isolated, e. g., neither side can be grounded or tied to a voltage by the customer

The dc voltage levels between the ranges of -6 v and -1 v will create an indeterminate condition which when addressed and sensed or read may result in a one or zero bit for that position in the word.

Read speeds up to 500,000 words per second are possible, but repetitive reading of the same group is conditioned by the filter. The filter and line capacities introduce a delay following a change in value before the system can reliably detect the new condition. The delay following voltage level input is 2.5 msec maximum before a reliable signal is obtained. If the voltage level input is turned off, a maximum delay of 5 msec will occur with line lengths up to 250 ft. The effect of increasing line capacitance is to lengthen the delay.

Adequate protection has been incorporated in this feature to prevent permanent damage to IBM equipment if 120 v ac is accidentally connected to a pair of customer input terminals.

A selective feature provides for a high repetitive reading speed for Digital registers. For example, telemetry registers may be coupled to the system using one or more modified voltage level groups, depending on register size and the number coding of the register. Conversion of the various number bases is accomplished via programming.

High-speed Telemetry Receiver registers may be read using the program mode of control (DPC) and an external interrupt for synchronization. Registers may be read using a Data Channel, synchronized by an external customer supplied sync signal.

Repetitive reading of the same group can proceed at rates up to 100,000 words per second. The specifications for each customer signal is up to 100 feet of customer twisted pair cabling from register to IBM terminations. The cabling should be so installed that it assures minimum noise.

Voltage levels:

Binary One: -1 v min to +30 v max
Binary Zero: -6 v min to -30 v max

Digital Input Channel

Process Operator Console (POC) input devices, such as decade switches and sense switches, and other low-speed inputs can be brought into the system by the formation of a Digital Input Channel using Electronic Contact Operate to select various groups of 16 bits over a single Digital Input group. POC input devices and cabling are handled via RPQ.

Pulse Counter Adapter

This feature is a prerequisite for adaption of pulse counters. This feature provides for a maximum

of 16 of the Pulse Counter feature. (Maximum - 8 Adapters per system.)

Pulse Counter

The Pulse Counter accepts discrete pulses as input information and advances by one per received pulse. The customer pulse is terminated by two-wire screw down termination at the individual counter terminal. These counters are read into the P-C in the same manner as a Digital Input group. Two counters are read from one address. The basic counter is an 8-bit binary counter. Two counters can be factory coupled together to obtain a 16-bit binary counter. The counters are reset when they are readout.

Maximum - 128 8-bit Pulse Counters per system.
Twisted pair input lines are recommended.
Pulse Rate: Not to exceed 5 kc. (Higher rates are possible with RPQ filters.)
Pulse Type: Same signal level requirements as Level Sense; the leading edge initiates the counts.
Pulse Form: Square Wave (minimum uptime 100 μsec, minimum downtime 100 μsec).

Process Interrupt Adapter

This feature (see Interrupt section of manual) is a prerequisite for adaption of Process Interrupts (Contact) and Process Interrupts (Voltage). Each Process Interrupt Adapter provides for 48 interrupt points. (Maximum - 8 Adapters per system)

Process Interrupt (Contact). Termination and sensing of 16 customer contacts associated with up to 4 levels of interrupt. (Maximum - 24 per system)

Process Interrupt (Voltage). Termination and sensing of 16 customer voltage levels associated with up to 4 levels of interrupt latches. (Maximum 24 per system)

Process inputs may be in the form of isolated dry contact closures, Process Interrupt (Contact), whereby IBM provides the sensing voltage for the contact, or in the form of a voltage level, Process Interrupt (Voltage). An interrupt is initiated by a contact closing, or a voltage level changing from 0 to 1 (0 if -30v to -6v and 1 if -1v to +30v). See the Interrupt section of the manual.

Digital Input Data Channel Adapter

This feature adapts digital input to a P-C Data Channel to enable digital input in the cycle stealing mode of operation.

External Sync

The Digital Input Data Channel Adapter provides this function: A "ready" condition is transmitted to an external device. The external device then provides a sync pulse which starts a cycle steal for reading a group of points. The sync pulse also turns off the ready condition. At the completion of the cycle steal operation, the ready condition is turned on again.

The ready condition down level is -12 volts through a 1,000 ohm resistor; the up level is between zero and -0.5 volt. The up level indicates the ready condition.

The customer generated sync pulse voltage levels must be between -6 and -18 volts for the down level and between -.35 and zero volts for the up level. The Digital Input Data Channel Adapter starts on a positive going transition.

The minimum positive pulse width is 2 μsec with a minimum down interval of 2 μsec before the next positive transition.

The signal must be transmitted on a single shielded conductor, which should be grounded at the Processor-Controller.

The Digital Input feature will be interlocked under External Sync until word count for last External Sync is obtained.

PROGRAMMED OPERATION

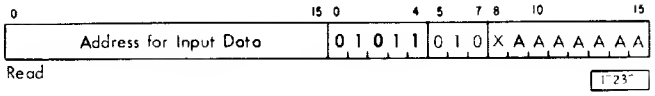
Digital input is processed by Direct Program Control (DPC) and/or the Data Channel (DC). When both operations exist, DPC may be used when the DC has completed its scan of the data table. The Digital Input Busy indicator is used to determine the status of the DC Program operation requires one XIO instruction for each Digital Input group (16 bits) to be transmitted to the Accumulator or core storage location. The DC operation requires one XIO instruction to initiate the transfer of a series of Digital Input groups in sequence. If a pulse counter is specified, the counter is reset.

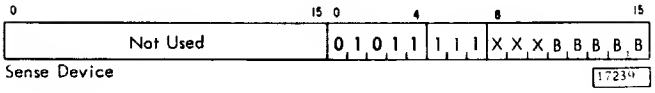
When Digital Input is under DPC, two XIO functions can be used. These functions perform the following operations:

READ	The Digital Input group addressed by the Modifier field is read into core storage.
SENSE	The Digital Input group (or Process Interrupt group) or the Device Status Word addressed by the Modifier field is placed in the Accumulator.

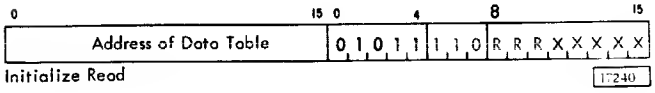
I/O CONTROL COMMANDS — DIGITAL INPUT

DIRECT PROGRAM CONTROL





DATA CHANNEL

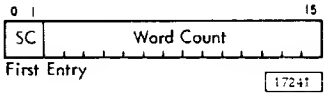


where:

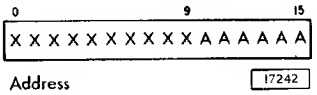
01011	is the assigned Area code for Digital Input
X	is not used.
AA...A	is the address of the Digital Input Group. These addresses range from 64_{10} through 127_{10}.
BBBBB	00000 and 00001 are the addresses of the Digital Input Device Status Word. The indicators are reset by 00001. Addresses 2_{10} through 25_{10} are assigned by the user to the Process Interrupt groups.
RRR	These bits have the following meaning: 000 Read Random 001 Read Sequential 010 Read Single Address 100 Read Random and External Sync 101 Read Sequential with External Sync 110 Read Single Address with External Sync

Interrupts and status indicators (modifier addresses 0_{10} through 25_{10}) may be read or sensed via DPC during a DC operation on Digital Input groups.

Data Table Formats



where SC are the Scan Control bits.

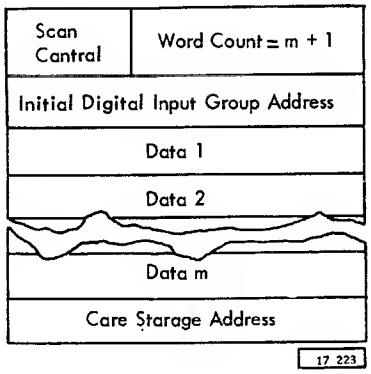


where X is not used and AA...A is the address of the Digital Input group. The first group has an address of 64_{10}, the 64th group has an address of 127_{10}.

Data Table Layouts

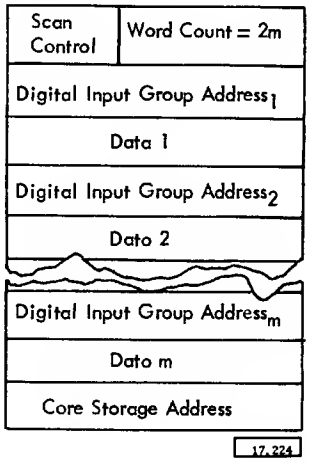
The Address field of the IOCC used with the Data Channel operation specifies the location of the first word of the table. There are several table layouts which are described below. The first word in the table contains the word count and the chaining control.

When operating in the Sequential or Single Address mode, the second word in the table contains the initial Digital Input group to be read into core storage, and the succeeding table locations receive the data read over a Data Channel as shown in the following table.



When READ Single Address is specified, the Initial Digital Input group is read over and over and placed in succeeding words of the table, until the word count reaches zero. When External Sync is specified, the cycle steal is initiated based on the External Sync pulse.

When operating in the Random mode, succeeding alternate words supply digital input addresses and receive data as shown in the following table.



When the word count reaches zero, normal Scan Control applies as described in the I/O Control section of the manual. An interrupt may be generated at the completion of the scan. The interrupt is called Digital Input Scan Complete.

TIMING: Digital Input groups will be read at the maximum rate of the channel unless a higher priority Data Channel request is honored, but timing restrictions due to filtering and customer load should be observed.

CAUTION: Chaining can lock out the P-C.

Device Status Word

An XIO Sense, specifying the Digital Input Area code (01011), includes the following indicators:

Parity — checks for odd bit parity during data transfers to and from core storage.
Storage Protect — turned on if an attempt is made to write into a "read only" location.
DI Scan Complete — Turned on and causes an interrupt when the word count goes to zero in a DC operation and the Scan Control bits specify an interrupt.
DI Busy — Turned on when DI is in use on a DC as the result of an XIO Initialize Read instruction. Turned off when the DC is not busy. An XIO (Read or Initialize Read) executed when this indication is on is ignored.

Digital Input (DI) Device Status Word Format:

Bit	Indicator Definition
0	Parity*
1	Storage Protect*
2	DI Scan Complete*
3-14	Not Used
15	DI Busy

*Causes an interrupt condition and turns on indicator. These must be on the same interrupt priority level.

The Digital and Analog Output (DAO) feature provides versatile control capability for the 1800 System. DAO features enable computer control over the many types of auxiliary devices required in a data acquisition or control system. Equipment that can be controlled includes set point positioners, displays, trend recorders, motor operated valves, and telemetry systems. The control outputs available with the DAO include the following:

1. Pulse Output (PO)
2. Electronic "Contact" Operate (ECO)
3. High-Speed Digital Register Output (RO)
4. High-Speed Analog Voltage Output (AO)

Pulse chaining and pulse-duration outputs are accomplished by programming.

The DAO features can communicate with the 1800 system via Direct Program Control (DPC) or a Data Channel (DC). A customer "external sync" pulse can be used to initiate DC operation.

Organization

The DAO features are organized as shown in Figure 35 and described below:

1. The 1800 Processor-Controller (P-C) provides the basic control for the DAO features.
2. The DAO Data Channel Adapter enables communication between the P-C and DAO devices via a Data Channel (maximum of one Data Channel Adapter per system).
3. The Digital Output Control and the Analog Output Control provide the interface between the P-C and the output registers. A maximum of eight Controls, in any combination, can be attached:
   a. Each Digital Output Control can accomodate 16 output registers. Note in Figure 35 that a Digital Output Adapter is required for each 4 output registers. (The Digital Output features may be installed in either the P-C or the 1826 Data Adapter Unit.)
   b. Each Analog Output Control can accommodate 8 Digital-to-Analog Converters. (The Analog Output features are connected to the Processor-Controller through 1856 Analog Output Terminals.)

External Sync (Electronic)

This function is provided by the DAO Data Channel Adapter feature. A ready condition is transmitted from the DAO feature to the customer's external device. The external device provides a sync pulse which starts a cycle steal for writing a group of points (DC operation).

The ready signal down level is -12v through a 1k ohm resistor, and the up level is between +0.0 and -0.5 volts. An up level indicates the ready condition. The sync pulse turns ready "off". At the completion of the cycle steal operation, the ready signal is turned "on" again.

The customer generated sync pulse voltage levels must be between -6 and -18 volts for the down level and between -0.5 and +0.5 volts for the up level. The Data Channel Adapter starts on a positive going transition. The minimum positive pulse width is 2 μsec, and the minimum down interval is 2 μsec before the next positive transition. The signals must be transmitted on a single shielded conductor which should be grounded at the P-C.

An "8-bit" in the modifier of an IOCC sets up the external sync mode. The absence of an "8-bit" in the modifier terminates the external sync mode.

System Capacity

The system capacity of DAO points depends on the combination of Digital Output (DO) and Analog Output (AO) points installed. Selection begins with the DO and AO Controls, maximum of eight:

1. If the maximum number of DO points are desired, eight DO Controls are installed. Each DO Control interfaces a maximum of four DO Adapters, providing a maximum of 32 DO Adapters. Each DO Adapter accomodates four 16-bit registers, maximum of 128 registers or 2048 bits. The installation of the DO maximum would eliminate the possibility of AO points.
2. If the maximum number of AO points are desired, eight AO Controls are installed. Each AO Control interfaces eight Digital-to-Analog Converters (DAC's), maximum of 64. Each DAC provides one or two AO points, depending on the DAC model. Thus a maximum number of 128 AO points can be installed. The installation of the AO maximum would eliminate the possibility of DO points.

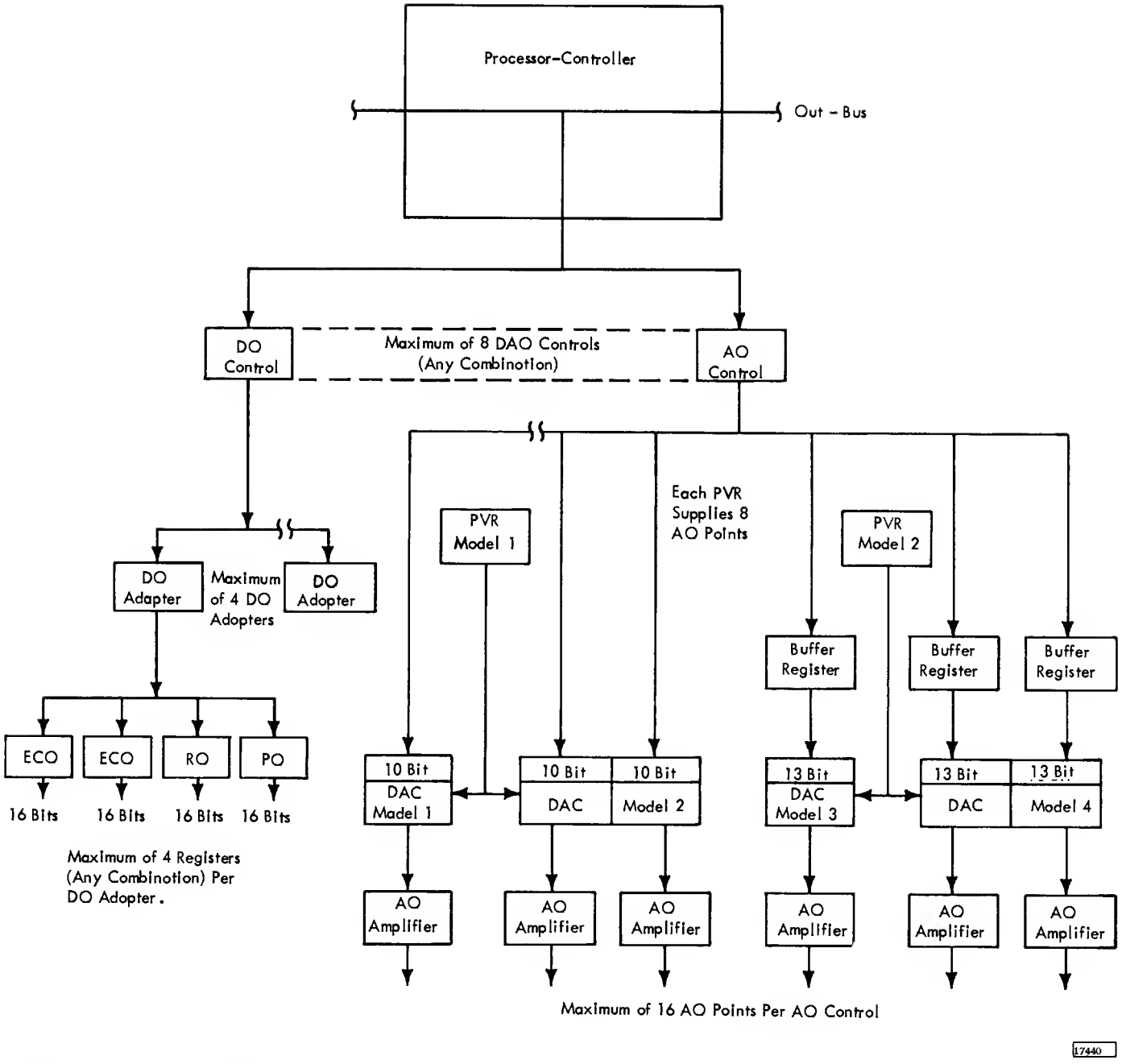


Figure 35. Schematic of Digital and Analog Output Features

Note that one AO point is equivalent to one 16-bit digital output register and that a total system limit of 128 AO points and/or DO registers exists.

This maximum of 128 is reduced when single point DAC's are installed. Each DAC Model 1 and 3 provides only one AO point, reducing the 128 maximum by one for each model 1 and 3 installed.

DIGITAL OUTPUT

Three types of digital output are available: Electronic "Contact" Operate, Pulse Output, and Register Output.

Electronic "Contact" Operate

ECO is used to operate alarms, console indicator lights and displays; and operating process equipment such as relays, conveyor belts, and pumps. Contact rating is 48 vdc at 0.45 amperes at distances up to 2500 ft. ECO's are provided in groups of 16 points (maximum 128 groups). The 16 points are set by a data transfer to the 16-bit register and remain latched until changed by another data transfer to the 16 bit register. A data bit of 1 corresponds to close (conducting) and a data bit of 0 corresponds to open (nonconducting).

Digital Output Channel: Process Operator Console (POC) output devices such as lights, digital displays and other low speed outputs can be operated by the formation of a "Digital Output Channel" using Electronic "Contact" Operate to select various groups of 16 bits over a single group of Electronic "Contact" Operate. POC Output devices and cabling are handled via RPQ.

Specifications:

Transfer Time (Resistive Load):	Less than 10 μsec turn on Less than 10 μsec turn off
Maximum Current Switched:	0.45 Amperes
Maximum Voltage (Positive voltage only):	+48 vdc (minimum +3 volts)

Customer supplied Power Supply.
Ground return for load current is common with system ground.

Load Characteristic: A wide variety of R, L, and C load characteristics can be accommodated within the above voltage and current specifications as long as the peak instantaneous voltage at the customer terminals does not exceed +65 volts or drop to less than -1 volt.

Pulse Output

The primary use of this output is to provide for pulse trains to operate such devices as latches, set point positioners, and other stepping motor devices. Pulse Outputs are provided in groups of 16 points (maximum 128 groups) and these are driven from each 16-bit register. The 16 points are momentarily switched by a data transfer to the 16-bit registers, and provide approximately 3 ms switching with a rating of 450 ma at 48 vdc. The ground return for the load current must be common with the system ground.

The outputs are "closed" immediately when the registers are loaded, and all are "opened" by the timing out of a 3-ms timer. The timer is started by using a separate XIO Control function so that the 3 ms pulse times out the reset of all pulse output points simultaneously. A data bit of 1 corresponds to closed (conducting) and a data bit of "0" corresponds to opened (nonconducting). Pulse chains are accomplished by programming.

Specifications for Pulse Output are similar to ECO except the duration of switch closure which is 3 ms minimum. When IBM Set Point Stations are driven with Pulse Output, a power terminal is provided on the 1801 or 1802 P-C.

Register Output

Digital data is transferred from core storage to the Register Output feature, maximum of 128 16-bit groups. The contents of each output register are then transmitted to customer-owned devices, such as telemeter registers, for a register to register transfer. Program control or a Data Channel operation can be used. The feature also has the ability to repeatedly write to a single register when using a Data Channel. The write can also be under the control of an external sync signal which generates a

signal to load new data into the register. The customer owned registers are then loaded by means of Register Output line drivers, with the following specifications:

Rate:	500,000 words (16 bits) per second maximum (to ensure this rate, the maximum distance of customer lines must be 100 feet or less)
Output Voltage:	binary "1" +3v (nominal) binary "0" 0v (nominal)
Output current available:	32 ma including termination and Customer supplied load. Termination and load returned to customer supplied +3 volts must present 100 ohms characteristic to transmission line.

ANALOG OUTPUT

There are two basic types of analog voltage outputs. The first type, DAC Models 1 and 2 (10 bit), is a fast response unipolar DAC utilizing digital storage of a single level. The second type, DAC Models 3 and 4 (13 bit), is a bipolar high speed, high accuracy DAC utilizing digital storage with a standard single level of buffering, and an option of double register buffering. Both types have the option of an Analog Output Driver Amplifier to provide low output impedance to match a wider variety of loads than the standard feature.

For both the 10-bit and 13-bit types, the Output Channel Register is force loaded to minimize DAC switching transients. This force loading means that the register goes directly from the previous value to the new value without being reset to zero in between.

DIGITAL-TO-ANALOG CONVERSION

There are four DAC Models:

1. Model 1 - Provides 10-bit digital-to-analog conversion for one analog output point.
2. Model 2 - Provides 10-bit conversion for two analog output points.
3. Model 3 - Provides 13-bit + sign conversion for one analog output point.
4. Model 4 - Provides 13-bit + sign conversion for two analog output points.

A Precision Voltage Reference, Model 1 or 2, is required to supply the DAC reference voltage.

DAC Models 1 and 2

DAC Models 1 and 2 provide unipolar analog output from 10-bit resolution, suitable for operating analog controllers, strip chart recorders, and other displays. Model 1 provides one analog output point, for a maximum of 64 points. Model 2 provides two output points, for a maximum of 128 points. The following list gives a summary of functional performance for this type of DAC, using the ±20 volt Precision Voltage Reference. (This performance will change when the Analog Output Driver Amplifier is used.)

Output Voltage:	+4.995 volts maximum
Input Data:	10 Bits
Output Impedance:	10K ohms
Resolution:	10 Bits
Conversion Time:*	6 μsec at customer termination

DAC Models 3 and 4

DAC Models 3 and 4 provide bipolar analog output from a resolution of 13 bits plus sign, suitable for hybrid systems. Negative numbers are handled in two's complement form. Model 3 provides one output point, for a maximum of 64 points. Model 4 provides 2 output points, for a maximum of 128 points.

The following list gives a summary of functional performance for this type of DAC, using ±20 volt Precision Voltage Reference. (This performance will change when the Analog Output Driver Amplifier is used.)

Output Voltage:	+4.9994 or -5.0000 full scale volts maximum
Input Data:	13 Bits + sign
Output Impedance:	10K ohms
Resolution:	13 Bits + sign
Conversion Time:*	6 μsec at customer termination

Buffer Register (DAC Models 3 and 4 Only)

It is frequently a requirement in hybrid computing and often an advantage in other applications to output several new values simultaneously. The Buffer Registers (one per analog output point) are loaded as the data is received from the P-C. An XIO Control instruction with a 9 bit is then executed to simultaneously load the analog output registers.

*With customer capacitive loads, response time is goverened by 10K output impedance and load capacitance.

Precision Voltage Reference (PVR)

The PVR feature is required to provide the precision voltage reference to the DAC. It is installed in the 1856 Analog Output Terminal; alternatively, the customer may supply his own precision voltage reference provided it meets the requirements of the DAC.

Each Precision Voltage Reference supplies eight analog output channels. The PVR Model 2 may be used with eight 10- or 13-bit resolution analog outputs when it is desired to mix the two kinds of outputs in a single terminal. It will be more economical, however, to use the 10-bit resolution PVR Model 1 for each full group of eight 10-bit output points.

Analog Output Driver Amplifier

The AO Driver Amplifiers provide 10 volt analog output and permit operation of AO points with a wide range of load impedances. The output impedance of the DAC's is 10K ohms. When it is desired to match loads differing greatly from this value, an output driver amplifier having an output impedance of less than 0.6 ohm may be used. This driver amplifier is applied on a per point basis to provide load impedance matching and voltage amplification. The driver amplifier will also be used when it is desired to increase the analog output voltage from its normal 5 volts to 10 volts. The use of the driver amplifier reduces the speed and accuracy somewhat. The following is a summary of analog output performance buffered by the amplifier and using the ±20 volt Precision Voltage Reference:

	DAC Models 1 and 2	DAC Models 3 and 4
Output voltage	+10 volts	±10 volts
Input data	10 bits	13 bits + sign
Minimum Load	1 K	1 K
Maximum Capacity Load	2000 picofarads	2000 picofarads
Output Impedance*	<0.6 ohm @ DC	<0.6 ohm @ DC
Resolution	10 bits	13 bits
Conversion Time**	20 μsec	20 μsec

*At customer terminals.

**With 1 K resistive load and 2000 picofarads capacitive load.

1856 Analog Output Terminals

There are two models of the 1856:

Model 1 provides power and housing for four DAC's--as many as eight AO points if only DAC Models 2 and 4 are installed; as few as four AO points if only DAC Models 1 and 3 are installed.

The 1856 Model 1 provides control circuitry for eight DAC's, any model. Thus a 1856 Model 1 is required for each multiple of eight DAC's.

Model 2 provides power and housing for four DAC's, any model. One 1856 Model 2 can be installed for each 1856 Model 1 when the additional AO points are required. An 1856 Model 2 cannot be installed without an 1856 Model 1.

A maximum of sixteen 1856's can be installed in a 1800 system.

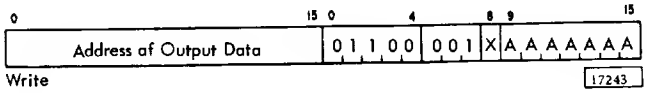
DAO PROGRAMMED OPERATION

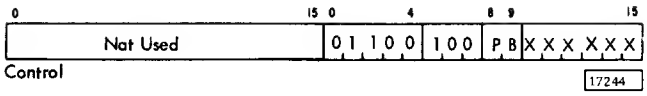
Digital and Analog Output (DAO) data are handled either by Direct Program Control (DPC) or Data Channel (DC) control. For DPC operation one Output Register is selected, and the digital data is transferred from core storage to the register of the output device using an XIO Write instruction. For DC operation a series of points are selected and data is transferred on a cycle steal basis using one XIO Initialize Write instruction to initiate the operation.

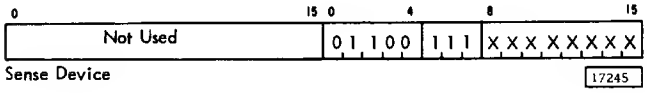
When both operations are used, program control operates when the DC has completed its scan of the data table. The DAO Busy indicator is used to determine the status.

I/O CONTROL COMMANDS - DIGITAL AND ANALOG OUTPUT

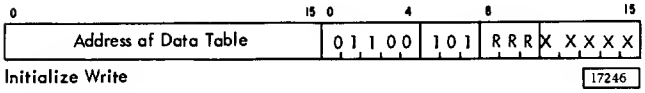
DIRECT PROGRAM CONTROL







DATA CHANNEL

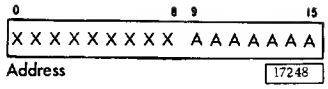


where:

01100	is the assigned Area code for Digital and Analog Output.
X	is not used.
AA...A	is the address of the digital or analog output register. The first register has an address of zero...the 128th register has an address of 127.
P	a one bit means initiate timing pulse on all Pulse Output points.
B	a one bit means initiate simultaneous transfer from Buffer Registers to all analog output points operating with the Buffer Register feature.
RRR	these bits have the following meaning: 000 - Write Random 010 - Write Single Address 100 - Write Random with External Sync 110 - Write Single Address with External Sync

DATA TABLE FORMATS

where SC are the Scan Control bits.



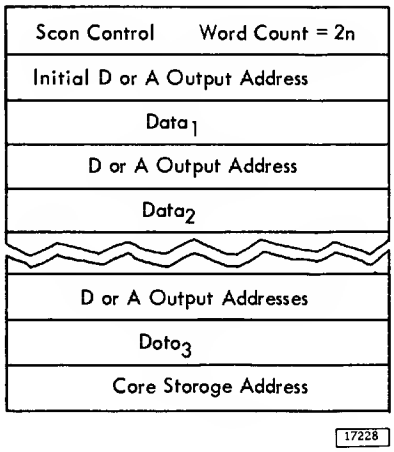
where X is not used and AA...A is the address of the digital or analog output register. The first register has an address of zero...the 128th register has an address of 127.

DATA TABLE LAYOUTS

The Address field of the IOCC used with Data Channel operation specifies the location of the first word of the table. There are several table layouts which are described below.

Write Random

When Write Random is specified, the first word in the table contains the word count (equal to two times the number of data words to be written) and the Scanning Control. The second word in the table contains the starting Digital or Analog Output address of the sequence of addresses to be scanned. The succeeding table locations contain the data to be converted and the DAO address, alternately, as shown in the following table:

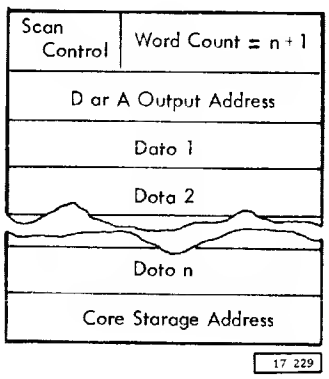


The total number of data and addresses transferred is specified by the word count. Data and Output Addresses are interleaved in the Table.

Write Single Address

When Write Single Address is specified, the word count equals the number of data words to be written

plus one. The Output point is written over and over with succeeding words of data from the table until the word reaches zero as shown in the following table:



When external sync is specified, the cycle steal is initiated based on the external sync pulse.

When the word count reaches zero, the normal Scan Control chaining applies as described in the I/O Control section of the manuals. An interrupt is generated at the completion of the scan. The interrupt is called DAO Complete.

TIMING: Digital Output words can be written up to the maximum rate of the channel. The actual output data rate to customer devices is limited by the device characteristics and the repetition rate to the same outputs or to single outputs. The rate can be controlled either by external synchronization or by programming, as specified by the output feature.

NOTE: Chaining can lock out the P-C.

Device Status Word

An XIO Sense, specifying the Area code of the DAO, includes the following indicators:

Parity - checks for odd bit parity during data transfers to and from core storage. Causes an interrupt.

Pulse Output Timer - indicator is on whenever the pulse output timer is on.

DAO Scan Complete - turned on and causes an interrupt when the word count goes to zero in a Data Channel operation and the scan control bits specify an interrupt; turned off by XIO Sense Device instruction.

DAO Busy - turned on when the Data Channel is in use as the result of an XIO Initialize Write; turned off when the Data Channel is not busy. Any XIO Write or XIO Initialize Write instructions executed when this indicator is on are ignored.

Digital and Analog Output Status Word Format:

Bit	Indicator Definition
0	Parity*
1	Pulse Output Timer
2	DAO Scan Complete*
3-14	Not used
15	DAO Busy

*Condition causes interrupt and turns on indicator. All DAO interrupts defined above must be of the same interrupt level priority.

The System/360 Adapter (located within the 1800 P-C) permits communication between the 1800 P-C and the System/360. Both systems regard each other as an I/O device capable of requesting service on a random basis. The System/360 Adapter is functionally equivalent to the corresponding System/360 device, the channel-to-channel adapter.

The channel provides the ability to transfer blocks of data and/or programs at rates up to 250 kb (kilobytes) between the System/360 and the 1800 System.

Addressing

The System/360 Adapter has two device addresses, one of which responds to the System/360 and the other to the 1800. This System/360 address is assigned at installation time. The 1800 is addressed with an area code of 01101. Each assignment conforms to the requirements of the two systems' channels.

Mode of Operation

The System/360 Adapter acts as a burst mode control unit on the System/360 channel and operates on a Data Channel with the 1800.

Data is transferred to or from the 1800, two 8-bit bytes at a time; data transfer to or from the System/360 channel occurs one 8-bit byte at a time. An 18-bit (16 data bits plus 2 parity bits) buffer register is provided for serializing and deserializing the data bytes. The left-hand byte of the buffer, corresponding to the more significant byte of the 1800 word, is loaded or transferred first over the System/360 channel.

The priority of the System/360 Adapter is selected for the 1800 by assigning a particular interrupt level and a particular Data Channel priority to the device. Control unit priority for the System/360 is governed by its position on the channel as defined in the IBM System/360 Principles of Operation Manual (A22-6821).

The System/360 Adapter provides Select Out Bypass to permit independent operation of the System/360 while the System/360 Adapter is inoperative.

COMMANDS

The System/360 Adapter decodes and responds to seven System/360 commands and four 1800 commands (See Table 8).

The Read, Read Backward, Write, and Control Immediate command bytes, including modifier bits, of the System/360 and the Initialize Read or Initialize Write control words of the 1800, after being presented to the idle Adapter, are available to the programmer of the other system by use of their respective Sense commands.

The M bit in the System/360 Read and Write commands, as shown below, will suppress the 1800 interrupt normally caused by a System/360 command when loaded into the buffer. For example, the program for a System/360 initiated transfer may involve first, a Control command which identifies the desired operation via the modifier bits, then a Read or Write to complete the operation. These may or may not be chained. Both commands could be latched in the Adapter buffer, and hence cause two interrupts in the 1800 System. The second interrupt (from the latched Read or Write command) would be caused if the 1800 System response to the indicated operation (coded in the Control modifier bits) were delayed, either by the interrupt being masked, or perhaps a required intervening Disk Storage Seek operation. Thus, at the time the command byte following the Control arrives at the Adapter from the System/360, the Adapter would be in an idle condition and would latch the second command in the Adapter buffer. This operation normally causes an 1800 System interrupt to establish the presence of a command byte. The M-bit modifier then, is provided to suppress the interrupt for a Read or Write which could cause unnecessary

Table 8. Commands

1800 System Commands			System/360 Commands	
Func.	Mod.			
101	XXXXXXXX	Initialize Write	Test I/O	XXXXX000
110	XXXXXXXX	Initialize Read	Write	XXXXXM01
111	00000000	Sense Device	Read	XXXXXM10
111	10000000	Sense Word Count	Control Immediate	XXXXX111
011	XXXXXXXX	Sense Interrupt Level	Sense	XXXX0 100
			Read Backward	XXXX1 100
			No Operation	XXXXX011

17 230

interrupts in an exchange sequence such as described above.

Stack Latch. A Stack latch is included in the Adapter so that if the System/360 wishes to stack Attention, Channel End, or Device End, it may do so by responding to Status-In with Command Out. Suppress Out may also be used to keep the channel from being overrun during chain data operations. or at any time the System/360 channel needs to slow the operation for some other reason. The System/360 Adapter will not request service from a channel while Suppress Out is up.

Device Status

System/360 Status Byte

The System/360 presents the following device status information to the System/360:

	System/360 Status Byte Bit Position
Attention	0
Busy	3
Channel End	4
Device End	5

The status definition and use of those bits presented to the System/360 are as defined in the System/360 Principles of Operation manual, Form A22-6821.

Attention. Indicates the condition, if on, that a prior read or write command function has been issued from the 1800 but has not yet been recognized by the System/360 channel.

Busy. The busy indication is off when the System/360 Adapter is idle. "Busy on" indicates that the device has been selected by the System/360 and either an operation is pending or a transfer is in progress.

Channel End. Presented to the System/360 channel during initial selection sequence for Control Immediate or No Op, or with Device End during the ending sequence for all others.

Device End. Presented to the System/360 channel during the initial selection sequence for No Op after either an 1800 Sense command response to Control Immediate, or at the end of the data transfer for all others.

1800 Device Status Word

The System/360 Adapter will present the following status information to a Sense command from the 1800:

	DSW Bit Position
Command Reject*	0
1800 Command Stored	1
360 Command Stored*	2
Halt*	3
Data Check*	4
Storage Protect*	5
Transfer End*	6
Not Used	7
360 Command Byte	8 - 15

* Interrupting Condition

Command Reject. This bit on indicates that the System/360 Adapter refused an 1800 command for one of the following reasons:

1. Invalid Op Code
2. An Initialize Read or Initialize Write was issued before a previous Initialize Read or Initialize Write had been cleared.
3. An Initialize Read was issued after the System/360 had issued a Read or Control command.
4. An Initialize Write was sent after the System/360 had issued a Write or Control command.

This bit causes an unconditional 1800 interrupt (unless masked) and is reset after an 1800 Sense with bit 8 off.

1800 Command Stored. This bit is on whenever the System/360 Adapter has accepted an Initialize Read or Initialize Write from the 1800. It is reset when Transfer End occurs.

360 Command Stored. This bit on indicates that the System/360 has issued a Read, Write or Control command which was accepted by the System/360

Adapter. If the command was Read or Write, this bit is reset when Transfer End occurs. If the command was Control, this bit is reset after an 1800 Sense with bit 8 off. An 1800 Sense command with bit 8 off or a complementary command will clear it as an interrupting condition.

Halt. This bit is turned on if the System/360 stops data transfer either with a normal stop or an interface disconnect sequence. Bit 6 (Transfer End) will also be on. This bit is reset after an 1800 Sense with bit 8 off.

Data Check. This bit on causes an unconditional interrupt in the 1800 (if not masked) and indicates that the 1800 detected a parity error during a cycle-steal. If the error was detected during the load word count cycle, the 1800 command registers are reset and the Transfer End bit is not turned on. The 360 portion of the Channel Adapter is unchanged (that is, any 360 command will remain latched and the 360 status is unchanged). If the parity error was detected during a data transfer cycle steal, an immediate ending procedure is initialized. The System/360 Adapter issues Device End and Channel End to the 360 and Transfer End to the 1800. This bit is reset by an 1800 Sense with bit 8 off.

If the channel detects incorrect parity during a control or data cycle, the channel adapter will ignore the command and will initiate No Interrupt to the 1800 or 360. (If the 1800 detects a parity error during the Control or Data cycles, a processor interrupt is caused.)

Storage Protect. This bit on indicates that the System/360 attempted to store data in a protected area in the 1800 memory on a 360 Write/1800 Read data cycle. This causes the System/360 Adapter to initiate an ending procedure, sending Channel End and Device End to the 360 and Transfer End to the 1800. An unconditional interrupt will be given to the 1800 (see Transfer End). This bit will be reset by an 1800 Sense with bit 8 off.

Transfer End. This bit on indicates that no additional data is to be transferred. This condition can be caused by the following conditions:

1. The 1800 Word Count goes to zero and no chaining is indicated.
2. The System/360 responds to Service In with Command Out.
3. The Systems/360 issues an interface disconnect sequence.
4. Parity is detected as described above.
5. A storage protect violation has occurred as described above.

Conditions 1, 2, and 3 may cause an 1800 interrupt if not suppressed by the Scan Control bits. Conditions 4 and 5 will cause an unconditional interrupt (if not masked).

This bit is reset by an 1800 Sense with bit 8 off. (An 1800 Initialize Read or Write will be rejected if the Transfer End status is on.)

360 Command Byte. If Bit 2 is on (360 Command stored) and Bit 1 is off (no 1800 command stored) bits 8 - 15 contain the issued 360 command byte (see Table 8).

Control Unit Priority

The priority of the System/360 Adapter is selected for the 1800 by assigning a particular interrupt level and a particular data channel priority to the device. Control unit priority for the System/360 is governed by its position on the channel as defined in the System/360 interface specifications.

Select Out Bypass

The System/360 Adapter will provide Select Out Bypass to permit independent operation of the System/360 while the Adapter is inoperative.

PROGRAMMED OPERATION

The System/360 Adapter performs with respect to the System/360 channel as described in the System/360 Principles of Operation manual with the exception described below.

The System/360 Sense command will store in memory at the address specified in the CCW up to two bytes of sense data under control of the byte count. The first byte contains the area and function of the 1800 control word from the high order byte of the System/360 Adapter buffer. The next byte, from the low order buffer byte, contains the modifier bits of that control word. All valid command codes from the System/360 are acceptable to the System/360 Adapter, hence undefined operations as established for each application will have to be rejected at the programming level in the 1800 P-C. The System/360 will reject undefined command functions from the 1800 and identify this occurrence by the Command Reject status bit presented in the device status word.

Other causes of command rejection and their identification are discussed in those sections where they would logically occur.

The following operations are explained using channel X to refer to the System/360 channel and channel Y for the 1800 channel.

CONTROL IMMEDIATE (System/360 Only)

Control as used in the System/360 Adapter is always an immediate command. This means that Channel End status is sent to channel X in response to the initial Command Out if the command is accepted, thus freeing the channel during the START I/O operation if a chain flag was not present. A Control from X may be rejected because Y had previously commanded the System/360 Adapter with an Initialize Read or Write.

The modifier bits in the Control command byte may be used to communicate the particular type of transfer requested by the System/360. The Control command is normally chained to a subsequent Read or Write command, depending on the operation necessary to complete the transfer.

Control to Idle Adapter: Channel X initiated the Control command. The complete command byte, including modifiers, is latched in the Adapter. The Adapter responds to the Command Out with Channel End status, thus freeing channel X, and initiates an interrupt in the 1800. The 1800, when interrupted, can accept the request by executing an XIO Sense command to the Adapter. The XIO Sense command loads into the 1800 accumulator the Device Status Word (DSW) containing the System/360 command byte from the buffer. A Device End status is then sent to the System/360.

Control to a Busy Adapter: A Control from channel X may be busied by one of three conditions:

1. The Control could be issued by channel X before a previous Control from channel X had been cleared. The Adapter response would be Busy status only.
2. The Control could be issued by channel X after a previous Control had been cleared but before the Device End had been accepted by channel X. The response would be Busy and Device End status. This would clear the Device End and leave the Adapter idle.
3. The Control might be issued by channel X after channel Y had issued an Initialize Read or Initialize Write command to the Adapter. The Adapter would respond with Busy and Attention status to channel X. The Attention, after being accepted in this way, would no longer attempt to get into the CPU, but if another command, such as Control, were issued from channel X, the response would still be Busy and Attention.

SENSE (System/360)

The Sense command is the normal response to a 1800 initiated transfer. When a Sense command is received by the Adapter, one or two 8-bit bytes with proper parity are transmitted to channel X. The sense bytes received by the channel consist of the contents of the Adapter buffer latches of the System/360 Adapter.

The Sense data presented under alternative conditions are:

Condition	High-Order Buffer BYTE 1	Low-Order Buffer BYTE 2
Adopter Idle	Zero	Zero
1800 Previously Issued:		
Initiolize Reod	Areo/Function	Modifier
Initiolize Write	Areo/Function	Modifier

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The only exception to the above is encountered when channel X issues a Sense command to the Adapter before a previous Control from channel X had been cleared. If the Control had not been answered by a Sense from channel Y, then the Sense Command Out would receive a Busy status in response. If the Control had been answered, but the Device-End had not been taken, or had been stacked, then the Sense Command Out would receive Busy and Device End status. This would clear the Device End from the Adapter.

SENSE (1800)

Three Sense commands are recognized by the Adapter when issued by the 1800 System. A Sense function executed by the 1800 channel will always present 16 bits of information which are placed in the accumulator.

Sense Device, Unmodified: When the control word bit 8 is equal to zero, the 1800 Device Status Word

is presented. The various conditions and the corresponding information appearing in the 1800 accumulator in response to the unmodified Sense function are shown as follows:

Condition	High-Order Accumulator	Low-Order Accumulator
Adapter Idle	Zero	Zero
Chonnel X has previously issued:		
Control, Read Backward, Read, Write	Device Status	Command Byte
HALT I/O	Device Status including Halt bit on	Zero
Transfer of Doto	Device Status, including bits 1 & 2 on	Data Byte from High-Order Buffer Byte
Channel Y previously issued:		
Initialize Reod, Initialize Write	Device Status including bit 1	IOCC Modifier

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The 1800 will always respond to the Adapter interrupt by executing a Sense command to identify the specific interrupting condition. Command bytes from the System/360 will appear as follows in the eight low-order bits of the accumulator. This command will reset all status bits except 1 and 2.

	8	9	10	11	12	13	14	15
Adapter Idle	0	0	0	0	0	0	0	0
Channel X has previously issued:								
Control	x	x	x	x	x	1	1	1
Read Backward	x	x	x	x	1	1	0	0
Read	x	x	x	x	x	M	1	0
Write	x	x	x	x	x	M	0	1

Sense Device, Modified (Sense Word Count): A modified Sense command ("one" in bit position 8 of the control word) is provided to present the current word count of the 1800 Data Channel.

Sense Interrupt Level. Identification of a particular interrupt on any level is accomplished with a Sense Interrupt Level command.

READ OR READ BACKWARD (System/360)

The Adapter controls recognize no difference between Read and Read Backward from channel X. In both cases, the primary function of the Adapter is the transmission of data bytes to channel X.

Read to an Idle Adapter: When the Read command is issued to an idle Adapter, channel X will receive an All-Zero status response and then will be held up until the other channel responds with an Initialize Write command. An interrupt is immediately set up to signal channel Y that an operation is waiting unless suppressed with the M bit. The complete Read command byte is latched in the Adapter buffer and is available to a Sense command from Channel Y.

Read to a Waiting Initialize Write: If a Read issued by channel X encounters a previously issued Initialize Write from channel Y, both operations will be performed. Channel X would receive Zero status in response to its Command Out whether the Attention had been accepted or not. The operation would continue until either channel X responded to its Service-In with a Command-Out Stop, or the Adapter WCR is zeroed, or both.

Upon receiving the Stop command from channel X, or the WCR is zeroed, a Status-In containing Channel End and Device End would be issued to channel X. If neither channel is chaining, then the acceptance of the status by channel X frees the Adapter and returns it to idle.

Read to a Busy Adapter: There are three Busy responses to a Read command issued by channel X:

1. Busy status alone would respond to the Command Out Read from channel X if channel X had previously issued a Control command that was still in the Adapter.
2. Busy and Device End status would be the response to a Command Out Read if a previously issued Control command had been cleared but the Device End had not been accepted. This would clear the Device End and leave the Adapter idle.
3. Busy and Attention status would be the response to a Command Out Read from channel X if channel Y had previously issued an Initialize Read. If the Attention had not been previously accepted by channel X, this would clear it as an interrupting condition, although it would still appear as a response to another Read until the previously issued command from channel Y was satisfied.

INITIALIZE READ (1800)

This command issued to a waiting Write command from the System/360 will initiate data transfer.

Initialize Read to Idle Adapter: Execution of this function latches the 16-bit portion of the IOCC containing the Area/Function/Modifier into the Adapter buffer, loads the Adapter word count, and raises Attention status to notify the System/360 that an operation is waiting.

Initialize Read to a Busy Adapter: There are two Busy responses to an Initialize Read command issued by channel Y:

1. Busy rejection is caused by issuing the command to a previously issued uncompleted command from the 1800. The condition can be interrogated with a Sense command which will indicate Command Reject status.
2. An Initialize Read to the Adapter, which contains a previously issued System/360 command byte other than Write, will be rejected.

WRITE (SYSTEM/360)

The primary function of the Adapter on a Write command is the acceptance of data from the writing channel for transmission to the reading channel.

Write to an Idle Adapter: When the Write command is issued to an idle Adapter, channel X will receive an All-Zero status response and will then be held up until the other channel responds with Initialize Read. An interrupt is immediately set up to signal channel Y that an operation is waiting if the interrupt has not been suppressed with the M bit. The complete Write command byte is latched in the Adapter and is available to a Sense command from the 1800.

Write to a Waiting Initialize Read: If a Write command issued by channel X encounters a previously issued Initialize Read from channel Y, both operations will be performed. Channel X would receive Zero status in response to its Command Out. The Operation would continue until channel X responded to a Service-In with a Command Out Stop or the Adapter word count was zeroed. Upon receiving the Stop command, a Status-In containing Channel End and Device End would be issued to channel X. If neither channel is chaining, then the acceptance of the status by channel X frees the Adapter and returns it to idle.

Write to a Busy Adapter: There are three Busy responses to a Write issued by channel X:

1. Busy status alone would respond to the Command Out Write from channel X if channel X had previously issued a Control command that was still in the Adapter.
2. Busy and Device End status would be the response to a Command Out Write if a previously issued Control command had been cleared but the Device End had not been accepted. This would clear the Device End and leave the Adapter idle.
3. Busy and Attention status would be the response to a Command Out Write from channel X if channel Y had previously issued an Initialize Write. If the Attention had not been previously accepted by channel X, this would clear it as an interrupting condition, although it would still appear as a response to another Write until the previously issued command from channel Y was satisfied.

INITIALIZE WRITE (1800)

Issued to a waiting Read command, Initialize Write initiates data transfer. If the Adapter is idle, Attention is triggered and the buffer is loaded with the function control word. Busy responses are as indicated under Initialize Read with the Read/Write relationships reversed.

TEST I/O (System/360)

A TEST I/O may be used by the programmer to determine the status of the System/360 Adapter any time the channel is free. The contents of the Adapter latches remain unchanged. The status received would indicate the condition of the Adapter as follows:

1. A Zero status would indicate that the Adapter was idle at the time of response.
2. A Busy status would indicate to channel X that a Control previously issued had not been accepted.
3. An Attention status would indicate to channel X that channel Y had previously issued an Initialize Read or Initialize Write.
4. A Device End status would indicate that a previously issued Control had been accepted, but that the final interrupting condition had not been accepted by the channel. This would clear the Device End status.

NO-OPERATION (System/360)

The No-Operation command as used with the System/360 Adapter does not affect the contents of the Adapter latches. It is always handled as an immediate command. Channel End and Device End are sent to channel X in response to the initial Command Out if the command is accepted. The No-Operation may be busy-rejected if there is outstanding status information held in the Adapter at the time the command is issued. The conditions for the busy-reject are described under "No Operation to a Busy Adapter," which is the second paragraph following.

No-Operation to an Idle Adapter: If a No-Operation is issued to an idle Adapter, channel X will receive a status response containing Channel End and Device End. No interrupt will occur in the 1800.

No-Operation to a Busy Adapter: A No-Operation from channel X may be busied by one of the following three conditions:

1. A No-Operation could be issued by channel X before a previous Control from channel X had been cleared. The Adapter response would be Busy status only.
2. A No-Operation could be issued by channel X after a previous Control had been cleared, but before Device End had been accepted by channel X. The response would be Busy and Device End. This would clear the Device End and leave the Adapter idle.
3. The No-Operation might be issued by channel X after channel Y had issued an Initialize Read, or Initialize Write command to the Adapter. The Adapter would respond with Busy and Attention status to channel X.

HALT I/O (System/360)

When an operating System/360 Adapter recognizes the HALT I/O condition, its response to the halting channel is immediate. It drops all "In" tag lines, sets Channel End and Device End in its status, and waits for a chance to send the status to channel X. If channel Y is operating with the Adapter, it receives HALT status via interrupt and a Sense command. If HALT I/O comes between Channel End and Device End, only Device End is presented. If HALT I/O comes after Device End has been accepted, no status is presented.

SELECTIVE RESET (SYSTEM/360) AND MASTER RESET (EITHER SYSTEM)

Either a selective reset or a master reset is handled like a Halt I/O with the single exception that no Channel End or Device End is sent to channel X, nor is an interrupt sent to the 1800. The Adapter is then not available to either channel for the duration of the reset (that is, while Operational Out is down).

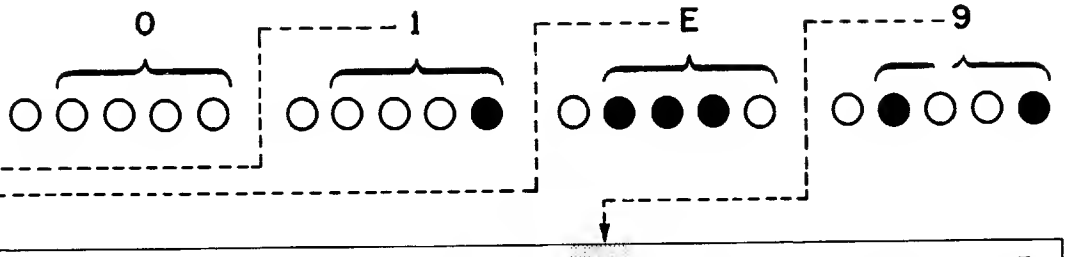
APPENDIX A. HEXADECIMAL-DECIMAL CONVERSION

The table in this appendix provides for direct conversion of decimal and hexadecimal numbers in these ranges:

HEXADECIMAL	DECIMAL
000 to FFF	0000 to 4095

For numbers outside the range of the table, add the following values to the table figures:

HEXADECIMAL	DECIMAL
1000	4096
2000	8192
3000	12288
4000	16384
5000	20480
6000	24576
7000	28672
8000	32768
9000	36864
A000	40960
B000	45056
C000	49152
D000	53248
E000	57344
F000	61440



	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00 _	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
01 _	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
02 _	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
03 _	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
04 _	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
05 _	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
06 _	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
07 _	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
08 _	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
09 _	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A _	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B _	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C _	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D _	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E _	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F _	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255
10 _	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
11 _	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
12 _	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
13 _	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
14 _	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
15 _	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
16 _	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
17 _	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
18 _	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
19 _	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A _	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B _	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C _	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D _	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E _	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F _	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511

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	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
20_	0512	0513	0514	0515	0516	0517	0518	0519	0520	0521	0522	0523	0524	0525	0526	0527
21_	0528	0529	0530	0531	0532	0533	0534	0535	0536	0537	0538	0539	0540	0541	0542	0543
22_	0544	0545	0546	0547	0548	0549	0550	0551	0552	0553	0554	0555	0556	0557	0558	0559
23_	0560	0561	0562	0563	0564	0565	0566	0567	0568	0569	0570	0571	0572	0573	0574	0575
24_	0576	0577	0578	0579	0580	0581	0582	0583	0584	0585	0586	0587	0588	0589	0590	0591
25_	0592	0593	0594	0595	0596	0597	0598	0599	0600	0601	0602	0603	0604	0605	0606	0607
26_	0608	0609	0610	0611	0612	0613	0614	0615	0616	0617	0618	0619	0620	0621	0622	0623
27_	0624	0625	0626	0627	0628	0629	0630	0631	0632	0633	0634	0635	0636	0637	0638	0639
28_	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
29_	0656	0657	0658	0659	0660	0661	0662	0663	0664	0665	0666	0667	0668	0669	0670	0671
2A_	0672	0673	0674	0675	0676	0677	0678	0679	0680	0681	0682	0683	0684	0685	0686	0687
2B_	0688	0689	0690	0691	0692	0693	0694	0695	0696	0697	0698	0699	0700	0701	0702	0703
2C_	0704	0705	0706	0707	0708	0709	0710	0711	0712	0713	0714	0715	0716	0717	0718	0719
2D_	0720	0721	0722	0723	0724	0725	0726	0727	0728	0729	0730	0731	0732	0733	0734	0735
2E_	0736	0737	0738	0739	0740	0741	0742	0743	0744	0745	0746	0747	0748	0749	0750	0751
2F_	0752	0753	0754	0755	0756	0757	0758	0759	0760	0761	0762	0763	0764	0765	0766	0767
30_	0768	0769	0770	0771	0772	0773	0774	0775	0776	0777	0778	0779	0780	0781	0782	0783
31_	0784	0785	0786	0787	0788	0789	0790	0791	0792	0793	0794	0795	0796	0797	0798	0799
32_	0800	0801	0802	0803	0804	0805	0806	0807	0808	0809	0810	0811	0812	0813	0814	0815
33_	0816	0817	0818	0819	0820	0821	0822	0823	0824	0825	0826	0827	0828	0829	0830	0831
34_	0832	0833	0834	0835	0836	0837	0838	0839	0840	0841	0842	0843	0844	0845	0846	0847
35_	0848	0849	0850	0851	0852	0853	0854	0855	0856	0857	0858	0859	0860	0861	0862	0863
36_	0864	0865	0866	0867	0868	0869	0870	0871	0872	0873	0874	0875	0876	0877	0878	0879
37_	0880	0881	0882	0883	0884	0885	0886	0887	0888	0889	0890	0891	0892	0893	0894	0895
38_	0896	0897	0898	0899	0900	0901	0902	0903	0904	0905	0906	0907	0908	0909	0910	0911
39_	0912	0913	0914	0915	0916	0917	0918	0919	0920	0921	0922	0923	0924	0925	0926	0927
3A_	0928	0929	0930	0931	0932	0933	0934	0935	0936	0937	0938	0939	0940	0941	0942	0943
3B_	0944	0945	0946	0947	0948	0949	0950	0951	0952	0953	0954	0955	0956	0957	0958	0959
3C_	0960	0961	0962	0963	0964	0965	0966	0967	0968	0969	0970	0971	0972	0973	0974	0975
3D_	0976	0977	0978	0979	0980	0981	0982	0983	0984	0985	0986	0987	0988	0989	0990	0991
3E_	0992	0993	0994	0995	0996	0997	0998	0999	1000	1001	1002	1003	1004	1005	1006	1007
3F_	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
40_	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
41_	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
42_	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
43_	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
44_	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
45_	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
46_	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
47_	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
48_	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
49_	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A_	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B_	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C_	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D_	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E_	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F_	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
50_	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
51_	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
52_	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
53_	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
54_	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
55_	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
56_	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
57_	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
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5A_	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
5B_	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C_	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D_	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E_	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F_	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535

11314

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61 _	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
62 _	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
63 _	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
64 _	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
65 _	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
66 _	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
67 _	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
68 _	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
69 _	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A _	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B _	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
6C _	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D _	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E _	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F _	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791
70 _	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
71 _	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
72 _	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
73 _	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
74 _	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
75 _	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
76 _	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
77 _	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
78 _	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935
79 _	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A _	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B _	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C _	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D _	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E _	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F _	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047

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80 _	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
81 _	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
82 _	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
83 _	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
84 _	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
85 _	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
86 _	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
87 _	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
88 _	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
89 _	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A _	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B _	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C _	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D _	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E _	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F _	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303
90 _	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
91 _	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
92 _	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
93 _	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
94 _	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
95 _	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399
96 _	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415
97 _	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431
98 _	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
99 _	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463
9A _	2464	2465	2466	2467	2468	2469	2470	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B _	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C _	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D _	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E _	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F _	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559

11315

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A0 _	2560	2561	2562	2563	2564	2565	2566	2567	2568	2569	2570	2571	2572	2573	2574	2575
A1 _	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A2 _	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A3 _	2608	2609	2610	2611	2612	2613	2614	2615	2616	2617	2618	2619	2620	2621	2622	2623
A4 _	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A5 _	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A6 _	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A7 _	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687
A8 _	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A9 _	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA _	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB _	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC _	2752	2753	2754	2755	2756	2757	2758	2759	2760	2761	2762	2763	2764	2765	2766	2767
AD _	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE _	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF _	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
B0 _	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B1 _	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B2 _	2848	2849	2850	2851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B3 _	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B4 _	2880	2881	2882	2883	2884	2885	2886	2887	2888	2889	2890	2891	2892	2893	2894	2895
B5 _	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B6 _	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B7 _	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B8 _	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B9 _	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA _	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB _	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC _	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD _	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE _	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF _	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071

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C0 _	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C1 _	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C2 _	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C3 _	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C4 _	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C5 _	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C6 _	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C7 _	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C8 _	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C9 _	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA _	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB _	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC _	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD _	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE _	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF _	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327
D0 _	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D1 _	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D2 _	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D3 _	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D4 _	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D5 _	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D6 _	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D7 _	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D8 _	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D9 _	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA _	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB _	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC _	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD _	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE _	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF _	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583

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	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E0_	3584	3585	3586	3587	3583	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E1_	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E2_	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E3_	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E4_	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E5_	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E6_	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E7_	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E8_	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E9_	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA_	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB_	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775
EC_	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED_	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE_	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF_	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839
F0_	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F1_	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F2_	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F3_	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F4_	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F5_	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F6_	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F7_	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F8_	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F9_	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA_	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB_	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC_	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD_	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE_	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF_	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

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Class	Instruction Name	Mnemonic	Hexadecimal
Load & Store	Load Accumulator	LD	C000
	Double Load	LDD	C800
	Store Accumulator	STO	D000
	Double Store	STD	D800
	Load Index	LDX	
	Disp into I		60xx
	Disp into XR1		61xx
	Disp into XR2		62xx
	Disp into XR3		63xx
	Addr into I		6400
	Addr into XR1		6500
	Addr into XR2		6600
	Addr into XR3		6700
	Contents (C) of Addr into I		64B0
	Contents (C) of Addr into XR1		65B0
	Contents (C) of Addr into XR2		66B0
	Contents (C) of Addr into XR3		67B0
	Store Index	STX	
	I stored at I+disp		6B00
	XR1 at I+disp		6900
	XR2 at I+disp		6A00
	XR3 at I+disp		6B00
	I stored at Addr		6C00
	XR1 stored at Addr		6D00
	XR2 stored at Addr		6E00
	XR3 stored at Addr		6F00
	I at C of Addr		6C80
	XR1 at C of Addr		6D80
	XR2 at C of Addr		6E80
	XR3 at C of Addr		6F80
	Store Status	STS	2800
	Clear Protect bit		2C40
	Set Protect bit		2C41
	Load Status	LDS	
	Set both Carry and Overflow off		2000
	Set Overflow on, Cry. Off		2001
	Set Carry on, Ofl. Off		2002
	Set both Carry & Overflow on		2003
Arithmetic	Add	A	8000
	Double Add	AD	8800
	Subtract	S	9000
	Double Subtract	SD	9800
	Multiply	M	A000
	Divide	D	A800
	Compare	CMP	B000
	Double Compare	DCM	B800
	Logical And	AND	E000
	Logical Or	OR	E800
	Exclusive Or	EOR	F000
Shift	Shift Left A	SLA	
	Shift Count (SC) in disp		10xx
	SC in XR1		1100
	SC in XR2		1200
	SC in XR3		1300
	Shift Left A & Q	SLT	
	SC in disp		10Bx
	SC in XR1		11B0
	SC in XR2		12B0
	SC in XR3		13B0
	Shift Left and Count A	SLCA	
	Shift Left A		104x
	SC in XR1		1140
	SC in XR2		1240
	SC in XR3		1340
	Shift Left and Count A & Q	SLC	
	SC in disp		10Cx
	SC in XR1		11C0
	SC in XR2		12C0
	SC in XR3		13C0
Shift	Shift Right A	SRA	
	SC in disp		180x
	SC in XR1		1900
	SC in XR2		1A00
	SC in XR3		1B00
	Shift Right A & Q	SRT	
	SC in disp		18Bx
	SC in XR1		1980
	SC in XR2		1A80
	SC in XR3		1B80
	Rotate Right A & Q	RTE	
	SC in disp		18Cx
	SC in XR1		19C0
	SC in XR2		1AC0
	SC in XR3		1BC0
Branch	Branch or Skip on Condition	BSC	
	Skip on any condition		48xx
	Br to addr on no cond		4C0x
	Br to XR1 + addr on no condition		4D0x
	Br to XR2 + addr on no condition		4E0x
	Br to XR3 + addr		4F0x
	Br to C of addr		4C8x
	Br to C of XR1 + addr		4D8x
	Br to C (XR2 + addr)		4E8x
	Br to C (XR3 + addr)		4F8x
	Branch and Store Instruction Counter	BSI	
	Br to EA + 1		40xx
	Br to EA + 1 on no condition		44xx
	Modify Index and Skip	MDX	
	Add disp to 1		70xx
	Add disp to XR1		71xx
	Add disp to XR2		72xx
	Add disp to XR3		73xx
	Add disp to addr		74xx
	Add addr to XR1		7500
	Add addr to XR2		7600
	Add addr to XR3		7700
	Add C (addr) to XR1		7580
	Add C (addr) to XR2		7680
	Add C (addr) to XR3		7780
Branch	Wait	WAIT	3000
I/O	Execute I/O	XIO	
	EA : disp + 1		08xx
	disp + XR1		09xx
	disp + XR2		0Axx
	disp + XR3		0Bxx
	addr		0C00
	addr + XR1		0D00
	addr + XR2		0E00
	addr + XR3		0F00
	C (addr)		0C80
	C (addr + XR1)		0D80
	C (addr + XR2)		0E80
	C (addr + XR3)		0F80

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APPENDIX C. INSTRUCTION EXECUTION TIMES

(The times below pertain to the 2 μsec core storage.
Add 2 μsec to Execution Times When Indirect Addressing is Specified)

	F = 0		F = 1	
	T=0	T≠0	T=0	T≠0
LD	4 1/4	4 1/4	6	6 1/4
STO	4 1/4	4 1/4	6	6 1/4
LDD	6 1/4	6 1/4	8	8 1/4
STD	6 1/4	6 1/4	8	8 1/4
A	4 1/2	4 1/2	6 1/4	6 1/2
S	4 1/2	4 1/2	6 1/4	6 1/2
AD	6 3/4	6 3/4	8 1/2	8 3/4
① SD	6 3/4	6 3/4	8 1/2	8 3/4
M	15 1/4	15 1/4	17	17 1/4
D	42 3/4	42 3/4	44	44 1/2
AND	4 1/4	4 1/4	6	6 1/4
OR	4 1/4	4 1/4	6	6 1/4
EOR	4 1/4	4 1/4	6	6 1/4
② BSI	2-4 1/4	2-4 1/4	2-6	2-6 1/4
② BSC	2	2	2-4	2-4 1/4
③ SLA	2 + N/4	2 + N/4	-	-
③ SLT	2 + N/4	2 + N/4	-	-
④ SLCA	2 + N/4	④ 2 1/2 + N/4	-	-
④ SLCAQ	2 + N/4	④ 2 1/2 + N/4	-	-
③ SRA	2 + N/4	2 + N/4	-	-
⑤ RTE	2 + N/4	2 + N/4	-	-
WAIT	2	2	2	2
⑥ XIO	6 1/4 - 8 1/4	6 1/4 - 8 1/4	8-10	8 1/4 - 10 1/4
LDX	2 1/4	2 1/4	6	6
STX	4 1/4	4 1/4	6	6
MDX	2 1/2	2 1/2	10 1/4	4 3/4
LDS	2	2	-	-
STS	4 1/4	4 1/4	6	6 1/4
① CMP	4 1/2	4 1/2	6 1/4	6 1/2
① DCM	6 3/4	6 3/4	8 1/2	8 3/4

① Execution Times Include an Average Add Time of 1 1/4 μsec.

② If a Skip or Branch is not Executed, the Instruction Performs as a NOP with an Execution Time of 2.0 us. If the Skip or Branch is Executed, the Second Execution Time is Applicable.

③ N = P-4, where P is the Number of Positions Shifted, and N must be Positive or Zero.

④ If T ≠ 0 and More Than Four (4) Shifts Occur, then 1/2 μs is Added to the Execution Time as Shown to Restore the Specified Index Register from the Shift Counter.

⑤ A Shift of 1, 2, 3 or 4 Positions Requires 2 μsec, with 1/4 μsec Added for Each Additional Shift Position up to 15. Therefore, a Shift of 5 Positions Takes 2.25 μsec, a shift of 6 Positions Takes 2.5 μsec, etc., up to 15 Positions which Takes 4.75 μsec.

A Shift of 16 Positions Requires 2.25 μsec, with 1/4 μsec Added for Each Additional Shift Position up to 31. Therefore, a Shift of 17 Positions Takes 2.5 μsec, a Shift of 18 Positions Takes 2.75 μsec, etc., up to 31 Positions Which Takes 6 μsec.

⑥ The longer times apply to the Read and Write functions, the shorter times to all other functions.

*Double these times for the 4 μsec core storage.

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Internal Add Operation

The arithmetic section of the 1801/1802 P-C performs additions in successive machine cycles that are 1/4 μsec (2 μsec core storage) or 1/2 μsec (4 μsec core storage) in duration. The number of machine cycles required to complete the addition depends on the numbers being added and the resulting "carries." As shown in Figure C-1, the augend

Machine Cycles	AUGEND (A-reg) and ANDEND (D-reg) Contents 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
	A_0 0 1 1 0 1 1 1 0 0 0 1 1 1 0 1 0
	D_0 1 1 1 1 0 0 1 1 0 0 0 1 1 1 0 1
*First	A_1 1 0 0 1 1 1 0 1 0 0 1 0 0 1 1 1
	D_1 1 1 0 0 0 1 0 0 0 0 1 1 0 0 0 0
*Second	A_2 0 1 0 1 1 0 0 1 0 0 0 1 0 1 1 1
	D_2 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0
*Third	A_3 0 1 0 1 0 0 0 1 0 1 0 1 0 1 1 1
	D_3 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
*Fourth	A_4 0 1 0 0 0 0 0 1 0 1 0 1 0 1 1 1
	D_4 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
**Fifth	A_5 0 1 1 0 0 0 0 1 0 1 0 1 0 1 1 1
	D_5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

*Occurs during the 2 or 4 μsec core storage cycle required to read the oddend from core staroge.

** Extro 1/4 or 1/2 μsec machine cycle. 17443

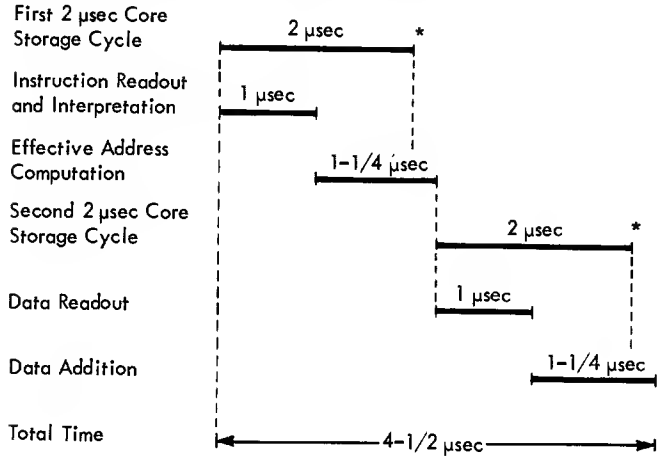
Figure C-1. Data Addition Example

(A register) and addend (D register) are "Exclusive Or'ed" and "And'ed" each machine cycle. (The Exclusive Or and And functions are explained in the Arithmetic Instructions section of the manual.) The results of the Exclusive Or function are placed in the A register. The results of the And function are ignored except for any carries that may occur. The carries are shifted one position to the left and placed in the D register. (These bits represent carries that would result from a normal binary add operation.) Each time a carry occurs, another machine cycle is initiated in which the A and D registers are Exclusive Or'ed and And'ed again. This process continues until there are no further carries, at which time the correct sum exists in the A register.

The length of each carry chain depends on the numbers involved and varies from 0 to 15. In Figure Ç-1, a carry chain of four (bit positions 2 through 5) caused five machine cycles. The first four of these cycles were included in the core storage cycle that read the addend from core storage. Only carry chain lengths of four and greater cause extra 1/4 or 1/2 μsec machine cycles.

Total Execution Time

Two core storage cycles are required in the execution of an Add instruction: one for instruction readout and effective address computation, and one for data readout and data addition. Figure C-2 is a sequence chart for the "average" add operation in which F = 0, T ≠ 0, and the carry chain length does not exceed four.



*Cycle steals can occur here without stopping effective address computation ar data additian. 17444

Figure C-2. Add Instruction Sequence Chart

Time Probabilities for the Addition of Data to the Accumulator

Table C-1 shows a mathematical analysis of all possible number pairs that can be added with the A and D registers:

Table C-1. Mathematicl Analysis of Addition of all Passible Number Pairs

Carry Chain Length	Probability (%)	Cumulative (%)	Time (μsec)
0	1.3363	1.3363	2.00
1	9.8892	11.2255	2.00
2	27.0115	38.2370	2.00
3	27.7178	65.9548	2.00
4	17.3702	83.3250	2.25
5	8.9237	92.2487	2.50
6	4.2404	96.4891	2.75
7	1.9485	98.4376	3.00
8	0.8789	99.3165	3.25
9	0.3906	99.7071	3.50
10	0.1709	99.8780	3.75
11	0.0732	99.9512	4.00
12	0.0305	99.9817	4.25
13	0.0122	99.9939	4.50
14	0.0046	99.9985	4.75
15	0.0015	100.0000	5.00

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The Carry Chain Length column lists all possible carry chain lengths up to the maximum of 15.

The Probability column contains percentage figures which are related to the Carry Chain Length. For example, a carry chain length of four occurs during 17.37% of all add operations.

The Cumulative column is merely a progressive summation of the Probability percentages. For example, 83.32% of all add operations involve carry chain lengths of four or less; which, incidentally, is the basis for the Average Execution Time given in this appendix for Add instructions.

The Time column shows the time required for Data Readout and Data Addition (see Figure C-2) with a 2 μsec core storage. The average Data Readout and Data Addition time for adding all possible numbers at random is 2.16 μsec.

The Area, Function, and Modifier codes listed below are required for 1800 I/O operations (x indicates an unused bit position):

	AREA	FUN	MODIFIER
Console Data Entry Switches			
Sense Device - switch data to A-reg.	0 0 0 0 0	1 1 1	0 1 0 x x x x x
Read - switch data to core.	0 0 0 0 0	0 1 0	0 1 0 x x x x x
Console Sense & Program Switches			
Sense Device - switch data to A-reg.	0 0 0 0 0	1 1 1	0 1 1 x x x x x
Read - switch data to core.	0 0 0 0 0	0 1 0	0 1 1 x x x x x
Console Interrupt			
Sense Device - console DSW to A-reg; indicators not reset	0 0 0 0 0	1 1 1	1 1 0 x x x x 0
- console DSW to A-reg; reset indicators	0 0 0 0 0	1 1 1	1 1 0 x x x x 1
Operations Monitor			
Control - timer not reset	0 0 0 0 0	1 0 0	1 1 1 x x x x 0
- reset timer	0 0 0 0 0	1 0 0	1 1 1 x x x x 1
Interval Timers			
Control - timers started or stopped according to bits 0-2 of IOCC first word.	0 0 0 0 0	1 0 0	0 0 1 x x x x x
Interrupt Mask Register			
Control - mask or unmask interrupt levels 1-14, depending on IOCC bit positions 0-13.	0 0 0 0 0	1 0 0	1 0 0 x x x x 0
- mask or unmask interrupt levels 15-24, depending on IOCC bit positions 0-9.	0 0 0 0 0	1 0 0	1 0 0 x x x x 1
Program Interrupt			
Control - turn on interrupt levels 1-14, depending on IOCC bit positions 0-13.	0 0 0 0 0	1 0 0	1 0 1 x x x x 0
- turn on interrupt levels 15-24, depending on IOCC bit positions 0-9.	0 0 0 0 0	1 0 0	1 0 1 x x x x 1

	AREA	FUN	MODIFIER
1053 Printer:			
First four 1053's:			
Write - individual 1053 specified by IOCC bits 11-14.	0 0 0 0 1	0 0 1	x x x y y y y x
Sense Device - 1053 DSW to A-reg. Individual 1053 specified by IOCC bits 11-14; bit 15 determines reset of indicators.	0 0 0 0 1	1 1 1	x x x y y y y y
Second four 1053's: Area code assigned by customer except where 1800 Time Sharing Executive program is used. Area code is then 01111.			
1816 Printer - Keyboard			
Read - single character to core storage.	0 0 0 0 1	0 1 0	x x x x 0 0 0 1
Sense Device - 1816 DWS to Accumulator. Individual 1816 specified by IOCC bits 11-14; bit 15 determines reset of indicators.	0 0 0 0 1	1 1 1	x 0 0 y y y y y
Control - places keyboard in Ready status.	0 0 0 0 1	1 0 0	x x x x 0 0 0 1
1442 Card Read - Punch			
First 1442:			
Initialize Read - card columns to core storage.	0 0 0 1 0	1 1 0	x x x x x x x x
Initialize Write - core storage to card columns.	0 0 0 1 0	1 0 1	x x x x x x x x
Control - IOCC bits 8-11 specify function.	0 0 0 1 0	1 0 0	y y y y x x x x
Sense Device - DSW to Accumulator.	0 0 0 1 0	1 1 1	x x x x x x x x
Second 1442: Area code assigned by customer except when 1800 Time Sharing Executive program is used. Area code is then 10001.			
1054 and 1055 Paper Tape			
Read - one character to core storage.	0 0 0 1 1	0 1 0	x x x x x x x x
Write - core storage to tape.	0 0 0 1 1	0 1 0	x x x x x x x x
Control - must precede Read.	0 0 0 1 1	1 0 0	x x x 1 x x x x
Sense Device - DSW to Accumulator.	0 0 0 1 1	1 1 1	x x x x x x x x

	AREA	FUN	MODIFIER
2310 Disk Storage Drive			
First 2310:			
Initialize Read-into-memory: yyy specify disk sector.	0 0 1 0 0	1 1 0	0 x x x x y y y
Initialize Read-check	0 0 1 0 0	1 1 0	1 x x x x y y y
Initialize Write	0 0 1 0 0	1 0 1	x x x x x y y y
Control - seek as specified by IOCC address.	0 0 1 0 0	1 0 0	x x x x x x x x
Sense Device - DSW to A-reg.	0 0 1 0 0	1 1 1	x x x x x x x x
Second and Third 2310's require Area codes of 01000 and 01001, respectively.			
1627 Plotter			
First 1627:			
Write - core storage to plotter.	0 0 1 0 1	0 0 1	x x x x x x x x
Sense Device - DSW to A-reg.	0 0 1 0 1	1 1 1	x x x x x x x x
Second 1627 Area code is assigned by user except when 1800 TSX program is used. Area code is then 10011.			
1443 Printer			
First 1443:			
Initialize Write - bit 15 is used for space suppress.	0 0 1 1 0	1 0 1	x x x x x x x y
Control - carriage control	0 0 1 1 0	1 0 0	x x x x x x x x
Sense Device - DSW to A-reg.	0 0 1 1 0	1 1 1	x x x x x x x x
Second 1443 Area code is assigned by user except when 1800 TSX program is used. Area code is then 10010.			
Analog Input			
Direct Program Control:			
Write - AI point to ADC; first word of IOCC is multiplexer address; where E is External Sync. L is 8-bit resolution. H is 14-bit resolution.	0 1 0 1 0	0 0 1	E x x L H x x x

	AREA	FUN	MODIFIER
Read - ADC to core storage; first word of IOCC is core storage address; where S is Sequential Program mode.	0 1 0 1 0	0 1 0	S x x x x x x x
Sense Device - DSW to A-reg; where C specifies Comparator or AI status word. R bit resets indicators.	0 1 0 1 0	1 1 1	C x x x x x x R
Data Channel Control:			
Initialize Read where T specifies a two DC operation.	0 1 0 1 0	1 1 0	E x T L H x x x
Initialize Write	0 1 0 1 0	1 0 1	x x x x x x x x

The AI Expander Area code is assigned by user except when the 1800 TSX program is used. Area code is then 10000.

Digital Input

Direct Program Control:			
Read - DI point to core storage; Bits 9-15 are DI addresses 64_{10} through 127_{10}.	0 1 0 1 1	0 1 0	x A A A A A A A
Sense Device - DSW or PISW to A-register; Bits 11-15 are either DSW addresses 00000 or 00001 (reset indicators) or PISW addresses 2_{10} through 25_{10}.	0 1 0 1 1	1 1 1	x x x B B B B B
Data Channel Control:			
Initialize Read - where bits 8-10 specify the read mode.	0 1 0 1 1	1 1 0	R R R x x x x x

Digital and Analog Output

Direct Program Control:			
Write - core storage to DAO device; where bits 9-15 are device addresses 0_{10} through 127_{10}.	0 1 1 0 0	0 0 1	x A A A A A A A
Control - where bit 10 initiates simultaneous transfer from buffer registers and bit 9 initiates timing pulse for Pulse Output.	0 1 1 0 0	1 0 0	P B x x x x x x
Sense Device - DSW to A-reg.	0 1 1 0 0	1 1 1	x x x x x x x x

	AREA	FUN	MODIFIER
Data Channel Control:			
Initialize Write - core storage to DAO registers. Bits 8-10 specify write mode.	0 1 1 0 0	1 0 1	R R R x x x x x
System/360 Adapter			
Initialize Write	0 1 1 0 1	1 0 1	x x x x x x x x
Initialize Read	0 1 1 0 1	1 1 0	x x x x x x x x
Sense Device	0 1 1 0 1	1 1 1	0 0 0 0 0 0 0 0
Sense Word Count	0 1 1 0 1	1 1 1	1 0 0 0 0 0 0 0
Sense Interrupt Level	0 1 1 0 1	0 1 1	x x x x x x x x
2401 or 2402 Magnetic Tape			
Initialize Read - where bits 10-15 specify: 10 Tape Unit 0 or 1. 11, 12 Bit density for 7-track. 13 "Packed-format" for 7-track. 14 Read-while-correcting. 15 Parity mode.	0 1 1 1 0	1 1 0	x x y y y y y y
Initialize Write - where modifier bits specify: 10 Tape Unit 0 or 1. 11, 12 Bit Density for 7-track. 13 "Packed-format" for 7-track. 15 Parity mode.	0 1 1 1 0	1 0 1	x x y y y y x y
Control - Bits 10-12 specify tape unit and bit density for 7-track:			
Rewind and unload	0 1 1 1 0	1 0 0	x x T D 0 0 0
Write tape mark	0 1 1 1 0	1 0 0	x x T D D 0 0 1
Erase	0 1 1 1 0	1 0 0	x x T D D 0 1 0
Backspace	0 1 1 1 0	1 0 0	x x T D D 0 1 1
Rewind	0 1 1 1 0	1 0 0	x x T D D 1 0 0
Sense Device			
Read DSW into A-reg.	0 1 1 1 0	1 1 1	0 x T x x x x 0
Read DSW and reset indicators	0 1 1 1 0	1 1 1	0 x T x x x x 1
Sense Channel Word Count	0 1 1 1 0	1 1 1	1 x x x x x x x

APPENDIX E. DEVICE STATUS WORDS

AREA	FEATURE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Consale Interrupt	* Interrupt Request															
	Interval Timers A-125μs, B-1ms, C-64ms	* Timer A	* Timer B	* Timer C													
1	1816 Printer - Keyboard	* Typewriter Service Request	* Keyboard Service Request	* Keyboard Request		Typewriter Busy	Typewriter Not Ready	Keyboard Not Ready	Storage Protect Violation	Keyboard Parity Error	Printer Parity Error			CE Busy	CE Not Ready		
	1053 Printer	* Service Request				Busy	Not Ready				Printer Pority Error			CE Busy	CE Not Ready		
2	1442 Card Read Punch			Error	Last Card	* Operation Complete	Parity Error	Storage Pratect Violation						CE Busy	CE Not Ready	Busy	Not Ready
3	1054/1055 Paper Tape Reader/Punch	Reader Any Error	* Reader Service Request	Punch Parity Error	* Punch Service Request	Reader Busy	Reader Not Ready	Punch Busy	Punch Not Ready	Reader Parity Error	Reader Storage Protect	CE Reader Busy	CE Reader Not Rdy	CE Punch Busy	CE Punch Not Rdy		
4	2310 Disk Storage	Any Error	* Operation Complete	Disk Not Ready	Disk Busy	Home	Parity Error	Storage Protect Violation	Data Error	Write Select	Data Overrun		CE Not Ready	CE Busy		Sector Count High	Sector Count Low
5	1627 Plotter	* Service Request	Parity Error											CE Busy	CE Not Ready	Busy	Not Ready
6	1443 Printer	* Transfer Complete	Error	* Printer Complete	Channel 9	Channel 12	Channel 1	Parity				CE Carriage Busy	CE Printer Busy	CE Not Ready	Carriage Busy	Printer Busy	Not Ready
10	Analog Input Basic	* End of Table	* DPC SS Conv Complete	* DPC Rly Conv Complete	* Storage Protect Violation	* Parity Control Error	* Parity Data Error	* ADC Overload	* Overlap Conflict	Cyc Steal, SS, ADC Busy	DPC Busy						Any Error
	Comparator	* High Out of Limit	* Low Out of Limit	* Overload	SS MPX			AMAR 512	AMAR 256	AMAR 128	AMAR 64	AMAR 32	AMAR 16	AMAR 8	AMAR 4	AMAR 2	AMAR
11	Digital Input Basic	* Parity Error	* Storage Protect Violation	* DI Scon Complete													DI Busy
	PISW	◄ Process Interrupt Points ►															
12	Digital and Analog Output Basic	* Pority Error	Pulse Output Timer	* D & A Out Scan Complete													D/AO Busy
14	2402 Mag Tape		Tape Unit Select	Command Reject	* End of Table	Chain Stop	Storage Protect Violation Stop	Tape Data Error	Parity Error	Data Overrun	* Operation Complete	Tape Diagnostic Error	Wrong Length Record	At Load Point	Tape Indicator or Mark	Tape Channel Busy or Rewind	Tape Channel Busy or Not Ready
13	S/360 Adopter	* Command Reject	1800 Command Stored	360 * Command Stored	* Holt	* Data Check	* Storage Protect	* Transfer End		◄ 360 Command ►							
	Adopter Word Counter	◄ Word Counter ►															

*Interrupt Conditions

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